1995-06

Harmonic distortion correction using active power line conditioners

Jones, Kevin David.

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

HARMONIC DISTORTION CORRECTION USING ACTIVE POWER LINE CONDITIONERS

by

Kevin David Jones

June 1995

Thesis Advisor: Robert W. Ashton

Approved for public release; distribution is unlimited

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 1995	Engineer's and Master's Thesis

4. TITLE AND SUBTITLE
HARMONIC DISTORTION CORRECTION USING ACTIVE POWER LINE CONDITIONERS

5. FUNDING NUMBERS

6. AUTHOR(S))
Kevin D. Jones

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey, Ca 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

Harmonic distortion of a voltage wave form on a local distribution system may have many effects, such as: protective device malfunctions, medical equipment failures, and increased noise generation and bearing wear of rotating equipment. In the past these effects have been tolerated. Advances in semiconductor technology in the past two decades have produced devices that can handle large amounts of power efficiently and safely. These advances have led to an increased number of loads that contribute to the bus voltage distortion.

These same advances that have made the distortion problem worse also have given rise to devices that can be used to actively correct the problem. Active Power Line Conditioners (APLC's) use voltage or current converters to improve harmonic distortion on local buses. APLC's use information from current or power sensors that are spread throughout the distribution system in order to correct the voltage wave form distortion. These sensors are difficult and costly to install. This thesis presents an APLC that produces its distortion canceling signal using only bus voltage information thus reducing the distribution sample points to one. The LabVIEW graphical programming language is used for sampling and control of the APLC

14. SUBJECT TERMS
Active Power Line Conditioner, Harmonic Distortion

15. NUMBER OF PAGES 61

16 PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

Standard Form 298 (Rev 2-89)
Prescribed by ANSI Std z39-18

Approved for public release; distribution is unlimited

HARMONIC DISTORTION CORRECTION USING ACTIVE POWER LINE CONDITIONERS

Kevin David Jones
Lieutenant, United States Navy
B.S., Oregon State University, 1988

Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER

and

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL

June 1995

Author: [redacted]
Kevin David Jones

Approved by: [redacted]
Robert W. Ashton, Thesis Advisor

[redacted]
Michael K. Shields, Second Reader

[redacted]
Michael A. Morgan, Chairman
Department of Electrical and Computer Engineering

ABSTRACT

Harmonic distortion of a voltage waveform on a local distribution system may have many effects, such as: protective device malfunctions, medical equipment failures, and increased noise generation and bearing wear of rotating equipment. In the past these effects have been tolerated. Advances in semiconductor technology in the past two decades have produced devices that can handle large amounts of power efficiently and safely. These advances have led to an increased number of loads that contribute to the bus voltage distortion.

These same advances that have made the distortion problem worse also have given rise to devices that can be used to actively correct the problem. Active Power Line Conditioners (APLC's) use voltage or current converters to improve harmonic distortion on local buses. APLC's use information from current or power sensors that are spread throughout the distribution system in order to correct the voltage waveform distortion. These sensors are difficult and costly to install. This thesis presents an APLC that produces its distortion canceling signal using only bus voltage information, thus reducing the distribution sample points to one. The LabVIEW graphical programming language is used for sampling and control of the APLC

TABLE OF CONTENTS

I. INTRODUCTION 1

II. DISTORTION SOLUTIONS 3

A. PREVENTION 3

B. ISOLATION 4

C. CORRECTION 4

1. Passive Correction 5

a. Line Reactors 5

b. Custom Designed Harmonic Filters (CDHF) 5

c. Isolation Transformers 7

2. Active Correction 7

III. ACTIVE POWER LINE CONDITIONER IMPLEMENTATION 9

A. NETWORK 10

B. CURRENT CONVERTER 11

C. A/D AND D/A CONVERTERS 13

D. CORRECTION SIGNAL 14

E. COMPUTER 16

IV. SOFTWARE IMPLEMENTATION 17

A. LABVIEW OVERVIEW 17

B. COMPUTER PROGRAM 17

1. Data Acquisition 19

2. Data Processing 20

3. Control Development 25

4. Signal Output 30

V. ACTIVE POWER LINE CONDITIONER TESTING AND RESULTS 33

A. TEST SETUP 33

B. RESULTS 36

VI. CONCLUSIONS AND RECOMMENDATIONS 47

A. CONCLUSIONS 47
B. RECOMMENDATIONS 47
LIST OF REFERENCES 49
INITIAL DISTRIBUTION LIST 51

ACKNOWLEDGMENT

Thank you to my Lord and Savior, Jesus Christ, who through his grace and mercy has sustained me.

To my family and friends in Christ a special thanks for your prayers and patience during difficult times.

I. INTRODUCTION

Electric power generation plants produce power generally in a sinusoidal fashion. The majority of the loads that are consuming this power are passive and nearly linear in nature. Non-linear loads, while they have existed for many years, have made up only a fraction of the power consumers on a distribution system and their undesirable effects have been tolerated. Technological advances in semiconductor devices are making these non-linear loads more prevalent.

Modern power electronic devices, such as the insulated-gate bipolar transistor (IGBT), power metal-oxide-semiconductor field effect transistor (MOSFET) and silicon-controlled rectifier (SCR), are capable of handling large amounts of electrical power efficiently and safely. Devices like these are finding more and more applications, such as light dimmers, AC/DC converters and adjustable speed motor drives. [Ref. 1] These applications have made life easier and made available the ability to perform a wider range of functions with existing electrical equipment. Many times the advantages of the improved electronics have an accompanying disadvantage; the use of power electronic devices has increased the percentage of power that is drawn in a non-linear fashion to the point where their effects may become unacceptable.

Non-linear power electronic loads draw currents that are not sinusoidal. These currents act in an Ohm's law relationship with the distribution systems' transformers and cables to cause distortion in the voltage of buses where the non-linear loads are connected. [Ref. 2] All loads attached to the bus are subject to the distorted voltage waveform and therefore may not operate as designed.

Distortion in the voltage waveform is defined as any deviation from the fundamental sinusoidal shape. The distorted waveform is periodic and therefore can be

represented by a Fourier series expansion. The magnitudes of the non-fundamental coefficients of the series expansion are a measure of the harmonic content of the distorted signal, hence the title "harmonic distortion".

The effects of the distorted voltage are wide ranging. Fault isolation devices, such as fuses and breakers, are sporadically interrupting power when no faults are present. Transformers and motor windings are overheating even though all parameters are within prescribed limits. Motor drives and computers are malfunctioning stopping critical computer-controlled processes and medical equipment [Ref. 1]. Variations in the electromagnetic torque developed by AC motors cause minute speed fluctuations leading to increased bearing wear and acoustic noise generation.

There are many approaches to the correction of this distortion. Chapter II provides a brief summary of the correction devices that have been and are being employed. The correction device designed and tested for this thesis is presented in Chapter III. The programming language and program used for information processing and control are described in Chapter IV. Chapter V contains the testing and results. The summary and recommendations are stated in Chapter VI.

II. DISTORTION SOLUTIONS

The problems that harmonics produce are as widespread as the techniques used to eliminate them. The troublesome harmonics are addressed in three ways: (1) prevent the production of harmonic distortion; (2) isolate the distortion from harmonic sensitive equipment , and; (3) correct the distortion.

A. PREVENTION

Power electronic devices such as AC-DC converters, while a major contributor to harmonic distortion, can be carefully controlled so that the distortion created is minimized. Depending on the control scheme used in the converter, particular harmonics can be eliminated altogether or higher harmonics produced instead. These higher harmonics are more easily filtered out by the distribution system itself without the use of additional filter devices.[Ref. 3] Active shaping of the input line current is one method used to minimize the harmonic production on the distribution systems. Figure 2.1 shows the basic wave shaping scheme. The step-up converter is operated in a current regulator mode and

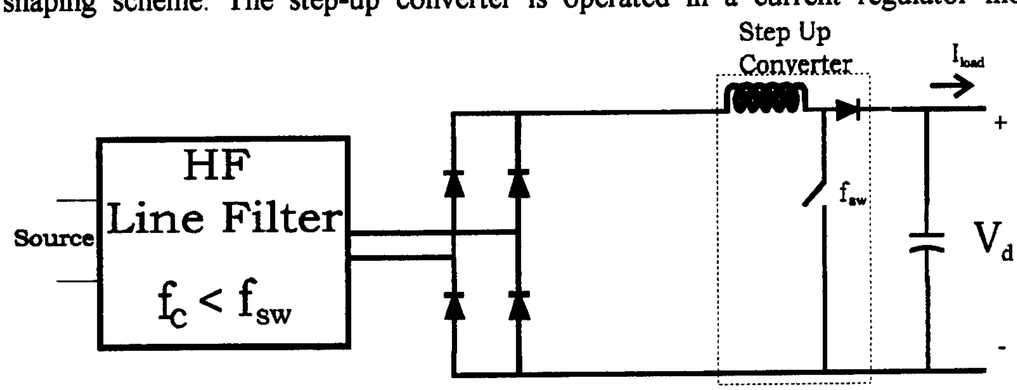

Figure 2.1 Wave Shaping Circuit

controlled such that the current drawn from the line is in phase with the voltage wave form and is sinusoidal. The switching frequency of the step-up converter is significantly higher than the harmonics that are being corrected. Even though the switching frequency effects will be seen in the line voltage they will be easily filtered by the transmission line inductance.

B. ISOLATION

On essential loads, such as medical equipment and critical process controlling computers, it is necessary at times to isolate them from a harmonically corrupt distribution system. Uninteruptible Power Supplies (UPS), though commonly used as a backup for power outages, are excellent for voltage regulation problems as well as suppressing incoming line transients and harmonic disturbances. [Ref. 3]

A block diagram showing how a UPS may be used to isolate distortion from critical loads is shown in Figure 2.2. As a harmonic isolation device, the UPS would be sensitive to the total harmonic distortion (THD) on the line side of the rectifier. When distortion of the line gets to the point where the critical load is affected the source of power to the load is shifted from the normal AC supply to the UPS output powered by the battery.

C. CORRECTION

In the event that harmonic distortion can not be prevented from occurring on a distribution system and cost limits the use of UPS's on all loads, then harmonic correction is the last resort. There are many ways to correct the harmonic distortion present on a given distribution system. The correction may be passive or active.

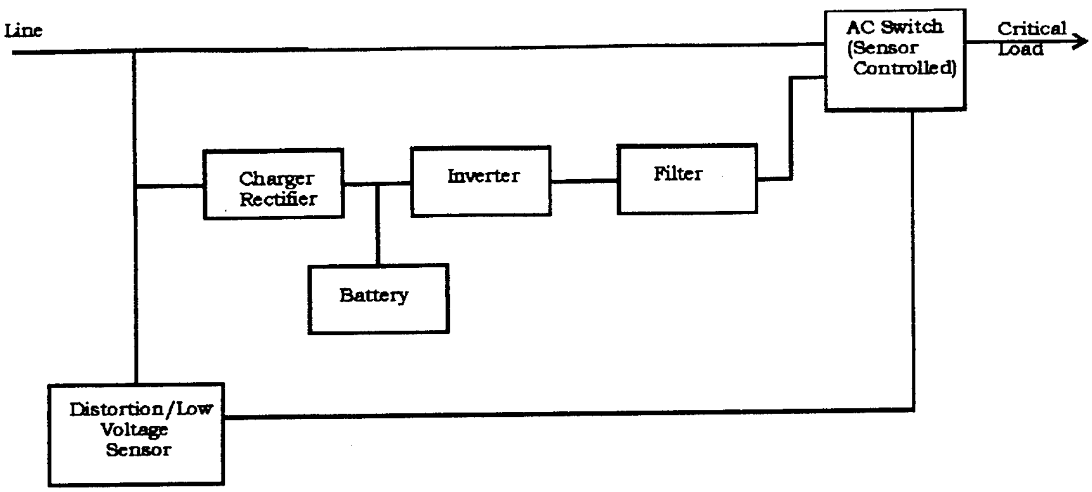

Figure 2.2 Isolation Block Diagram

1. Passive Correction

On many devices passive elements are added in series with the load in order to filter the harmonics or minimize the damage from the distortion.

a. Line Reactors

The simplest passive filter used is an inductor connected in series with the harmonically corrupting load, Figure 2.3. The increased inductance, due to the line reactor, results in a higher effective value of the AC inductance which improves the power factor and reduces harmonics.[Ref. 3] This method is cheap but inefficient because of the considerable losses in the inductor.

b. Custom Designed Harmonic Filters (CDHF)

An extension of the line reactor is the addition of shunt capacitors in order to make band pass filters, Figure 2.4. The filters are tunable to the harmonic frequency to be attenuated. The ability to tune the filter to remove selected harmonics improves correction system flexibility. However these tuned filters are susceptible to detuning due

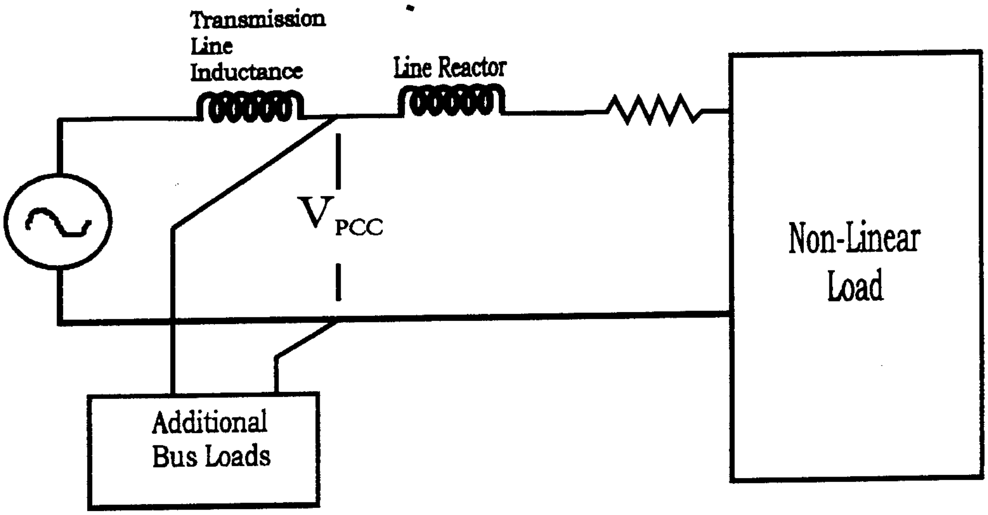

Figure 2.3 Line Reactor

to aging and temperature variations thus removing their effectiveness. Effectiveness may also be eliminated if the distribution configuration causes the harmonic footprint to change. Harmonics not originally accounted for may not be filtered. In addition, distribution configuration changes or harmonic generated by remotely located nonlinear loads within the filter's bandwidth, may sink into it causing an overload condition.

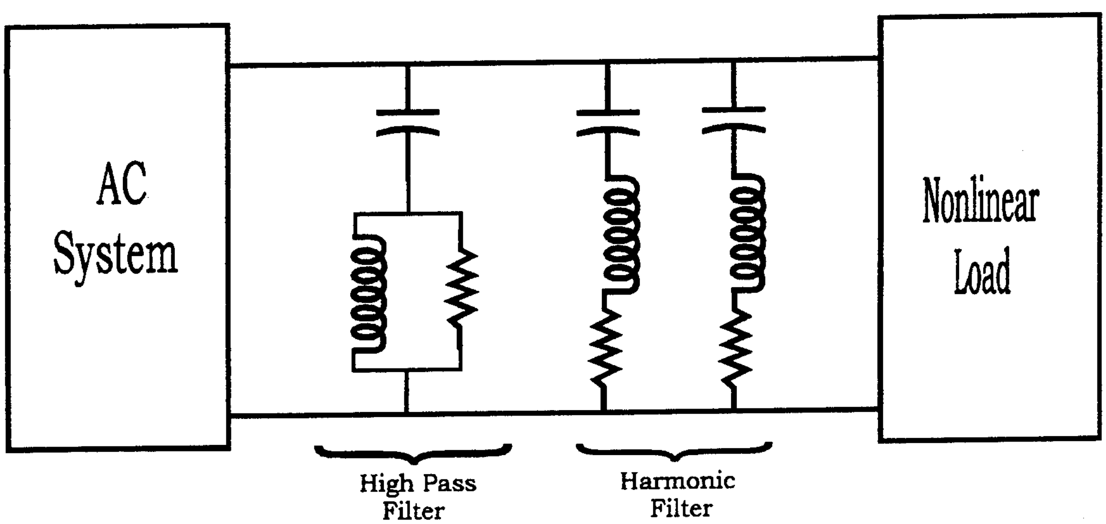

Figure 2.4 Custom Designed Harmonic Filter

c. Isolation Transformers

Zig-Zag or Wye-Delta transformers trap zero sequence harmonics such as 3,6,9 etc. The isolation comes at the expense of increased losses in the transformers. The harmonics create a significant amount of eddy current losses within the transformer that has caused transformers to literally explode from overheating. Recently "K-rated" transformers have emerged with a greater ability to withstand the additional stress damage and overheating.[Ref. 4] The "K factor" is simply a de-rating factor of the transformer.

2. Active Correction

The voltage wave form at a given node may be distorted or additionally distorted by drawing non-linear current from that node. A "stiff" system is one in which the voltage at that bus is not sensitive to the current flowing through it. While a "weak" system is one where the bus voltage is quite sensitive to the current. Whether a given bus is "stiff" or "weak" is generally described by its short circuit current. The higher the short circuit current the stiffer the bus. Provided that the system is not to "stiff" the bus voltage can be realistically corrected by injecting current into the node with the proper magnitude and phase angle.[Ref. 1] This is precisely what an Active Power Line Conditioner (APLC) attempts to accomplish.

Active power line conditioners can be broadly categorized by the type of converter used, voltage or current, and the domain in which correction occurs, time or frequency. DC to AC converters are dc supplies connected to an inverter which is switched in many different fashions to create a desired wave shape. The inverter alternately switches between positive, negative and common terminals in order to supply or absorb power as needed. Voltage or current converters differ primarily by their dc source. The voltage converter dc supply consists of a capacitor which resists a change in voltage where a

current converter's supply is an inductor which resists a change in current. Figure 2.5 shows a basic voltage and current converter. [Ref. 1]

Correction in the time domain is based on adjusting the instantaneous voltage or current wave shape to that of a reference. An error function is developed by comparing the measured voltage or current wave shape to a template. The error function then provides the needed control information to the converter controlling the injected current or output voltage. [Ref. 1]

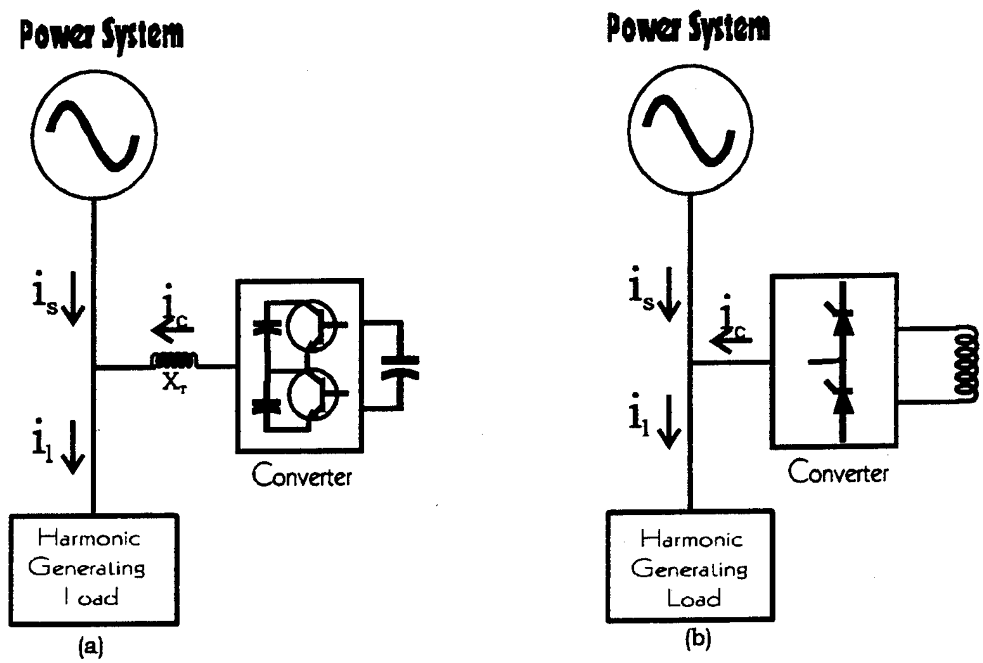

Figure 2.5 Voltage (a) and Current (b) Converter

Frequency domain correction is based on determining the harmonic content of the distribution system waveform. The Fourier transform of the waveform yields the energy content of the harmonics. Once the Fourier transform is taken, the inverter switching function is determined to develop the distortion-canceling wave shape.[Ref. 1]

III. ACTIVE POWER LINE CONDITIONER IMPLEMENTATION

The active power line conditioner implemented in this thesis used a frequency domain correction controlling a current converter. The APLC, Figure 3.1, is made up of the network, current amplifier, D/A and A/D converters, correction signal and computer.

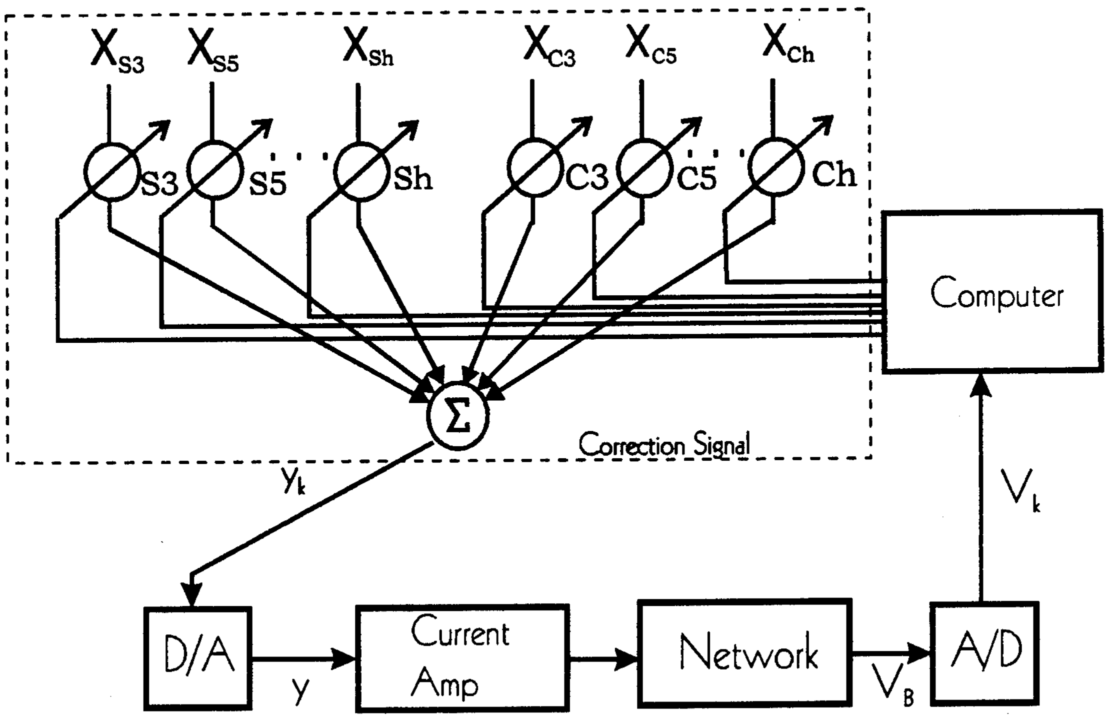

Figure 3.1 Active Power Line Conditioner

The network is made up of the distribution system seen at the node where the distorted voltage is to be corrected. The computer processes the sampled voltage wave form of the network to produce the desired weights that are applied to the harmonic sinusoids of the correction signal. The digital correction signal is the sum of the individual harmonic correction signals. The current amplifier amplifies the distortion-canceling wave

waveform that has been converted to an analog signal. The D/A and A/D converters allow interfacing between the analog network and digital processing equipment.

A. NETWORK

The node that the converter is connected to is the point of common coupling (PCC) between it and the distribution system. The network is what the converter sees looking into the distribution system at the PCC. The network is made up of linear and non-linear loads distributed throughout the power system. The voltage of the network is related to the impedance of the network by

$$v_{Bh} = \sum_{h=1}^{M} Z_{Bh} \; I_h \qquad 3.1$$

where v_{Bh} is the h harmonic component of the voltage at bus B,
Z_{Bh} is the impedance at bus B seen by harmonic current I_h,
M is the maximum harmonic number considered significant.

The network along with the a Norton equivalent circuit is depicted in Figure 3.2. The bus equivalent load is the linearized model about a particular harmonic current.

When the line conditioner is operating, the harmonic voltage at bus B, Figure 3.2b, is

$$v_B = v_1 + v_h + v_c \qquad 3.2$$

where $v_1 = V_1\sqrt{2}\,\sin(\omega \;\; t)$, fundamental voltage.
v_h is the voltage produced by the harmonic current.
v_c is the voltage produced by the conditioner current.

Equation 3.1 is a linear view of the voltage at the bus because in practice the impedance matrix that relates the harmonic current to the bus voltage can be significantly

coupled. The complex impedance in equation 3.1 is a function of the harmonic frequencies and currents. Coupling does not invalidate equation 3.2 but it makes the process of finding the correct harmonic currents to inject, such that v_h equals $-v_c$, difficult.

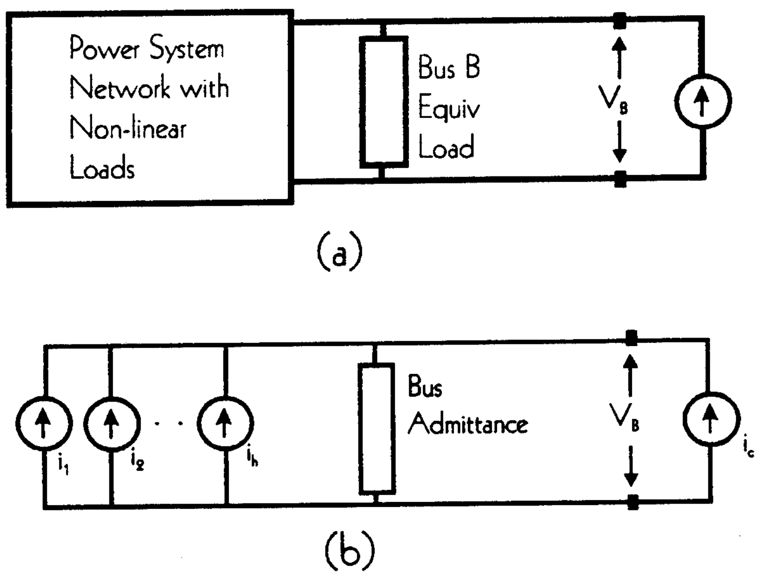

Figure 3.2 Network (a) and Norton Equivalent (b)

B. CURRENT CONVERTER

The converter used in the APLC is a model 262V pulse width modulated power amplifier manufactured by Copley Controls Corporation. A block diagram of the amplifier setup is shown in figure 3.3. The amplifier rails require an ungrounded voltage of 85 to 350 VDC. [Ref. 5]

The source is 208 VAC three phase which is made adjustable from zero to maximum by the variac and ground isolated by the Wye-Wye connected transformer. The ungrounded signal is rectified by the a three phase bridge rectifier and filtered to produce the needed rail voltage.

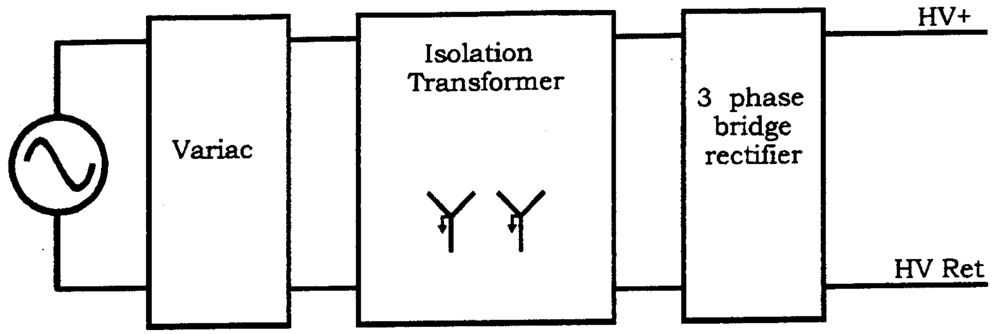

Figure 3.3 Amplifier Power Supply Block Diagram

The amplifier output signal is produced by alternately switching between the HV+ and HV Ret. The amplifier switching circuit is shown in Figure 3.4. Each set of switches

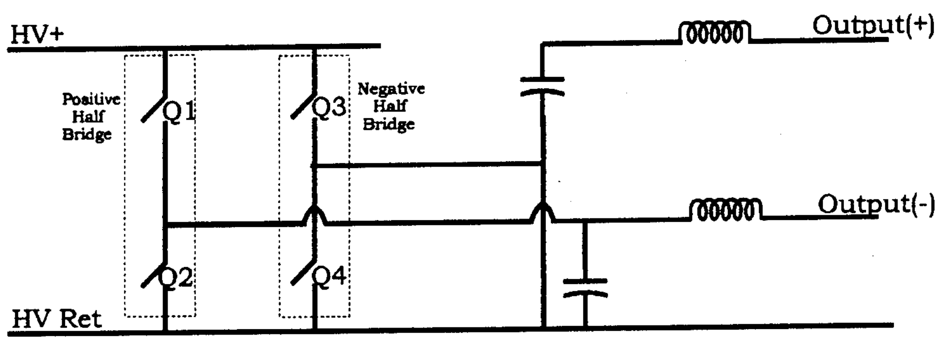

Figure 3.4 Amplifier Switching Circuit

(Q1, Q2 and Q3, Q4) constitute a half bridge power stage. The output (+) and the output (-) are either connected to the HV+ or HV Ret at all times. The average DC value at either output connection is a function of the voltage at HV+ and the duty cycle of the half bridge. The two half bridges continually have the same duty cycle, which is dictated by the input differential signal, but when the positive half bridge is connected to the HV+ the negative half bridge is connected to HV Ret. If the input signal is positive going then the duty cycle increases from 50% which produces a positive going voltage between output (+) and output (-). The duty cycle is 50% when the input is zero and the average DC voltage at the output will be zero. A negative going waveform at the input causes the

duty cycle to drop below 50% which produces a negative average DC voltage at the output. The output waveform is fedback and compared to the desired wave shape. This comparison is used to develop the control for the pulse width modulator. The pulse width modulator operates at 81 kHz. The output of the half bridges is a chopped DC voltage. A low pass filter at the output of the switches has a center frequency of 13.8 kHz and attenuates the 81 kHz ripple to approximately 2.0% of the maximum DC output. [Ref. 5]

The 262V amplifier was configured by the manufacturer to operate as a current amplifier from 0 to 5 kHz with an expected load inductance of 4 mH and a center frequency of 1.5 kHz. An inductor was added at the output to ensure that the amplifier would operate as a current source at frequencies as low as 60 Hz.[Ref. 5]

C. A/D AND D/A CONVERTERS

The A/D converter (ADC) is a 12 bit, sampling, successive approximation converter. The ADC has two input ranges that are software sellectable: -5 to 5 VDC or 0 to 10 VDC. The sampling rate is programmable up to 200 kHz and is independent of the host computer clock. Conversion data is stored in a dedicated buffer to accommodate differences in software and hardware speeds.[Ref. 6]

The D/A converter (DAC) is a 12 bit converter with an analog output range of 0 to 9.9976 V in steps of 2.44 mV for unipolar operation and -10 to 9.9951 V in steps of 4.48 mV for bipolar operation.[Ref. 6] The time of conversion is programmable to be either:

1. Convert immediately upon writing to the DAC register,
2. Convert when triggered by an external source, or
3. Convert when triggered by an internal strobe.

D. CORRECTION SIGNAL

The adaptively controlled correction signal is developed by the computer using a measure of total harmonic distortion (THD) as an error function. The error of this distorted signal is its departure from the fundamental waveform, equation 3.3. The waveform

$$e = v_B - v_1 \qquad 3.3$$

distortion is quantized by the Mean Square Error (MSE). It can be shown that

$$\varepsilon = E\left\{e^2\right\} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\alpha+2\pi} e^2 \, d\omega\, t} \qquad 3.4$$

Further, it can be shown that,

$$THD = \frac{\varepsilon}{V_1} \qquad 3.5$$

thus the MSE is minimized when the *THD* is minimized.

The correction signal components $x_{s3}, x_{s5} \cdots x_{sh}$ and $x_{c3}, x_{c5} \cdots x_{ch}$ are discrete versions of the harmonics detected in the bus voltage, as expressed in these equations.[Ref. 7]

$$x_{sh} = \sin\left(\frac{hk\omega T}{N}\right) \qquad 3.6$$

$$x_{ch} = \cos\left(\frac{hk\omega T}{N}\right) \qquad 3.7$$

where $h = 3,5$. ,
k is the time index,
$T = 1/f = 2\pi/\omega$ = cycle period,
N = number of samples per cycle.

The impedance matrix of the distribution system is unknown, implying that the amplitude and phase of the harmonic currents are also unknown. Based on this, the discrete signals were given an amplitude of one and phase of zero. The discrete signals are multiplied by weighting factors s_h and c_h then summed together to produce the desired discrete correction signal. [Ref. 7]

$$y_k = \sum_{\substack{h=odd \\ h\neq 1}} \left[s_h \sin\left(\frac{hk\omega T}{N}\right) + c_h \cos\left(\frac{hk\omega T}{N}\right) \right] \tag{3.8}$$

The determination of the weights are done with the help of the THD measurement. Equations 3.9 and 3.10 show the relationship between successive weights.

$$s_{k+1} = s_k + \left(-\nabla_s\right)\mu \tag{3.9}$$

$$c_{k+1} = c_k + \left(-\nabla_c\right)\mu \tag{3.10}$$

where $\nabla_s = \dfrac{\partial\, THD}{\partial\, s}$; $\nabla_c = \dfrac{\partial\, THD}{\partial\, c}$

The gradients of the *THD* and step size, μ, determine the rate of convergence. Figure 3.5 is used to illustrate this point. The *THD* surface is drawn as a function of one weight. The gradient of the surface points in the correct direction to minimize the *THD*, equation 3.11.

$$\nabla_c = {(THD_{k+1} - THD_k)}\Big/{(c_{k+1} - c_k)} \tag{3.11}$$

Since the sine and cosine functions are orthogonal functions, the weighing and summing process will eventually provide the missing amplitude and phase information to the distortion-canceling signal.

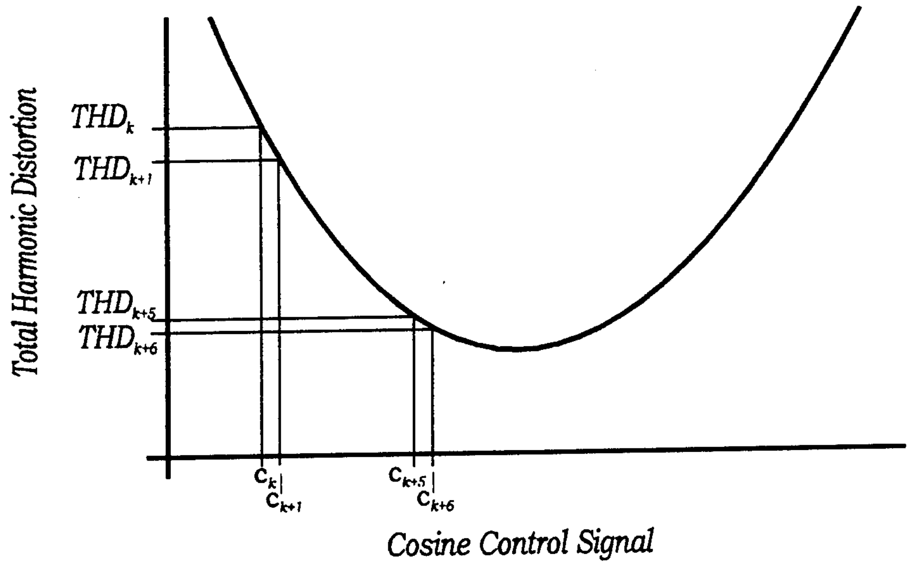

Figure 3.5 Example of One Weight Error Surface

E. COMPUTER

The computer used in the APLC is a DataStor 486-66. The computer is an IBM compatible AT with an EISA local bus. The computer houses the National Instrument AT-MIO-64F-5 data acquisition board. The AT-MIO-64F-5 is a high performance, multifunction analog, digital, and timing I/O board. The ADC and DAC reside on the board along with eight lines of TLL-compatible digital input and output, and three 16-bit counter/timer channels for timing input and output.[Ref. 8] The algorithm used by the computer for processing the input information and determining output signal was written in LabVIEW which is discussed in the next chapter.

IV. SOFTWARE IMPLEMENTATION

A. LABVIEW OVERVIEW

LabVIEW, like C and BASIC, is a program development application. Traditional programming has been done in text based languages. The growing trend is to object or graphically oriented languages, such as LabVIEW. Terminology, icons and ideas familiar to scientists and engineers are implemented in LabVIEW using graphical symbols rather than textual language. LabVIEW has extensive libraries of functions and subroutines that cover most programming tasks. Data acquisition, analysis, presentation and storage and GPIB and serial instrument control are among some of the existing libraries.[Ref. 9]

Programs developed in LabVIEW are called *virtual instruments* (VI's) because their appearance imitates that of actual instruments. VI's that are called by the running VI are called subVI's. The user interface portion of a VI is called the *front panel* and the source code equivalent is called the *block diagram*. The control switches and knobs and display gauges and graphs are contained in the *front panel*. Instrument control is performed using the keyboard or mouse. Instructions are executed in the *block diagram* which is actually a pictorial solution to the programming problem.[Ref. 9]

B. COMPUTER PROGRAM

The program developed for the APLC is called *HARMONIC.VI*, Figure 4.1 shows the front panel of this VI. The program consists of four main parts: 1. Data acquisition 2. Data processing 3. Control Development and 4. Signal Output. This section will discuss the theory behind and then the actual LabVIEW implementation of these program elements.

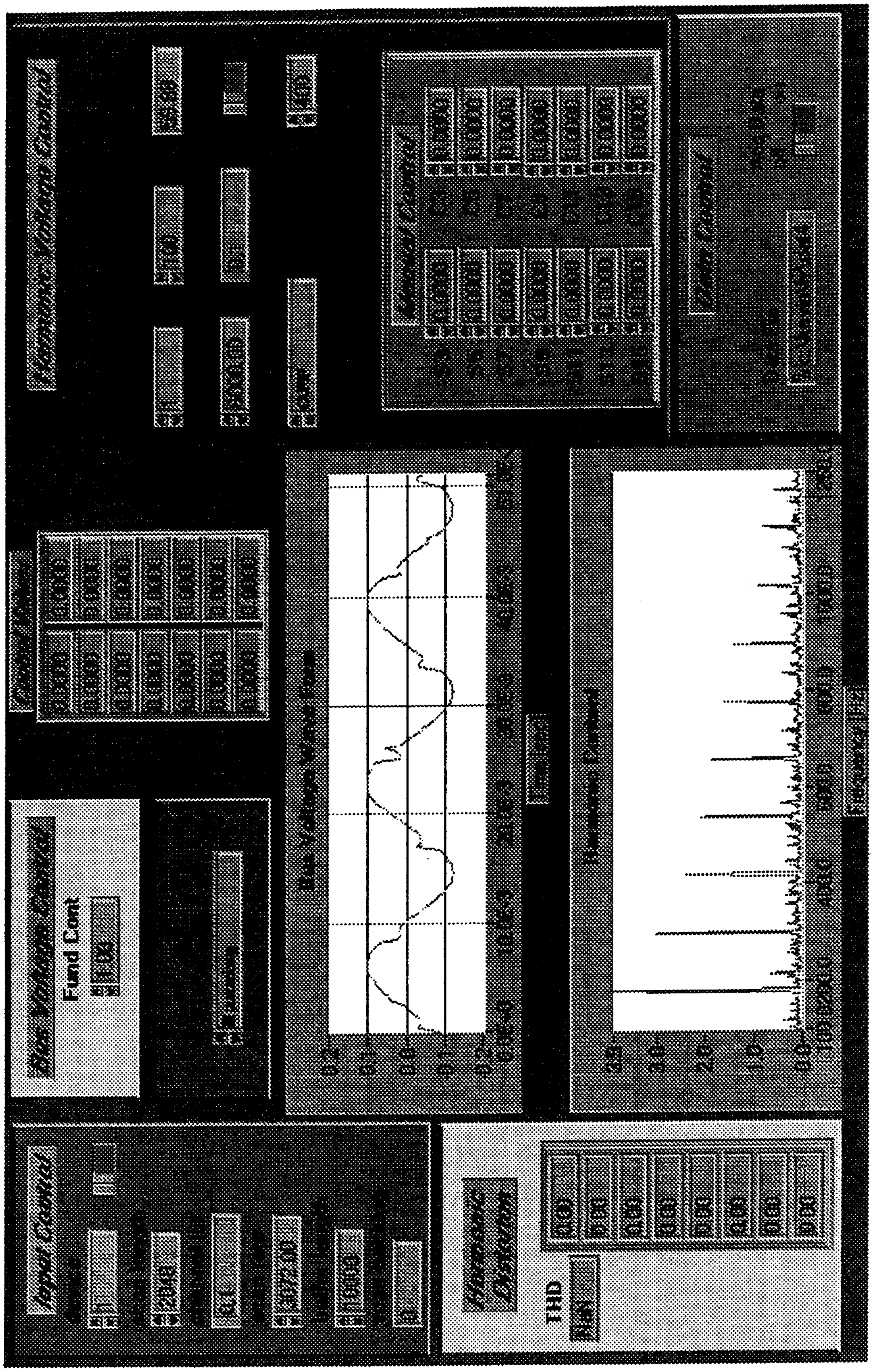

Figure 4.1. HARMONIC.VI Front Panel

1. Data Acquisition

Data acquisition is the process of sampling a signal and organizing the collected data in an useful format. The *HARMONIC.VI* controlled the data acquisition boards' parameters in order to meet the following:

1. The minimum sampling frequency must meet the Nyquist criteria. The expected analog signal to be sampled was a harmonically distorted sinusoid with a fundamental frequency of 60 Hz. It was decided that harmonics higher than the 21st would be negligible and that it would be considered the maximum signal frequency. The minimum sampling frequency is 2520 Hz.

2. The maximum sampling frequency was set by the programs ability to process the data. The sampled data is placed into a circular buffer of finite length. Contiguous segments of data are pulled off the buffer to be processed. If the processing rate is smaller than the sampling rate then the buffer over flows. This high limit for sampling frequency was empirically determined to be approximately 4000 Hz.

3. The scan length or record length is the specified amount of sampled data that is taken from the input buffer each cycle. The Fourier transform needed to be taken in the processing section each cycle therefore the record length was chosen to be the highest integer power of two that would not cause an input buffer overflow. The power of two facilitated the use of fast Fourier transform (FFT) algorithms to compute the discrete Fourier transform (DFT) which are more efficient and save processing time. The record length was set at 2048.

Any sampling frequency meeting the above criteria would work for the program. The final setpoint for the sampling frequency was 3072 Hz. This particular value was chosen to ensure that the frequency represented by the DFT would be near the fundamental and harmonic frequencies to minimize leakage. Figure 4.2. shows the block

diagram of the input while loop. The AI CONFIG, AI START and AI READ subVI's in conjunction with the while loop made up the data acquisition portion of *HARMONIC.VI*.

2. Data Processing

The purpose of the data processing section of the *HARMONIC.VI* was to take the 2048 element array of data provided by the data acquisition section and produce useful information for control and display. The processing section is shown in Figure 4.2 and is composed of the windowing case statement, DFT, THD and HARM AVE subVIs.

The array of data is a sampled rectangular windowed segment of the analog signal. The rectangular window arises from the finite record length of the array and creates undesired effects in the output of the DFT. The Fourier transform of the signal of interest x(t) is the sum of the delta functions at the harmonic frequencies.

$$\Im\{x(t)\} = X(f) = \sum_k A_k \delta(f - k f_1). \qquad 4.1$$

The actual data array has a finite record length, and is thus the continuous signal multiplied by a rectangle window function w(t). The Fourier transform of the resulting array is

$$\Im\{x'(t)\} = \Im\{x(t)w(t)\} = X(f) * W(f) = \sum_k A_k W(f - k f_1). \qquad 4.2$$

This is the convolution of X(f) and W(f). From this it is apparent that the impulses of the actual transform has been spread by the transform of the window function. The Fourier transform of the rectangle window is a *sinc* function. As the record length decreases the width of the zero crossings of this *sinc* function increases. For a given record length, the width of the zero crossings (and thus how much the impulses of the original signal's transform are spread) can be narrowed by using a digital window that tapers at the edges of the record. LabVIEW offers many types of windows of which the tapered cosine,

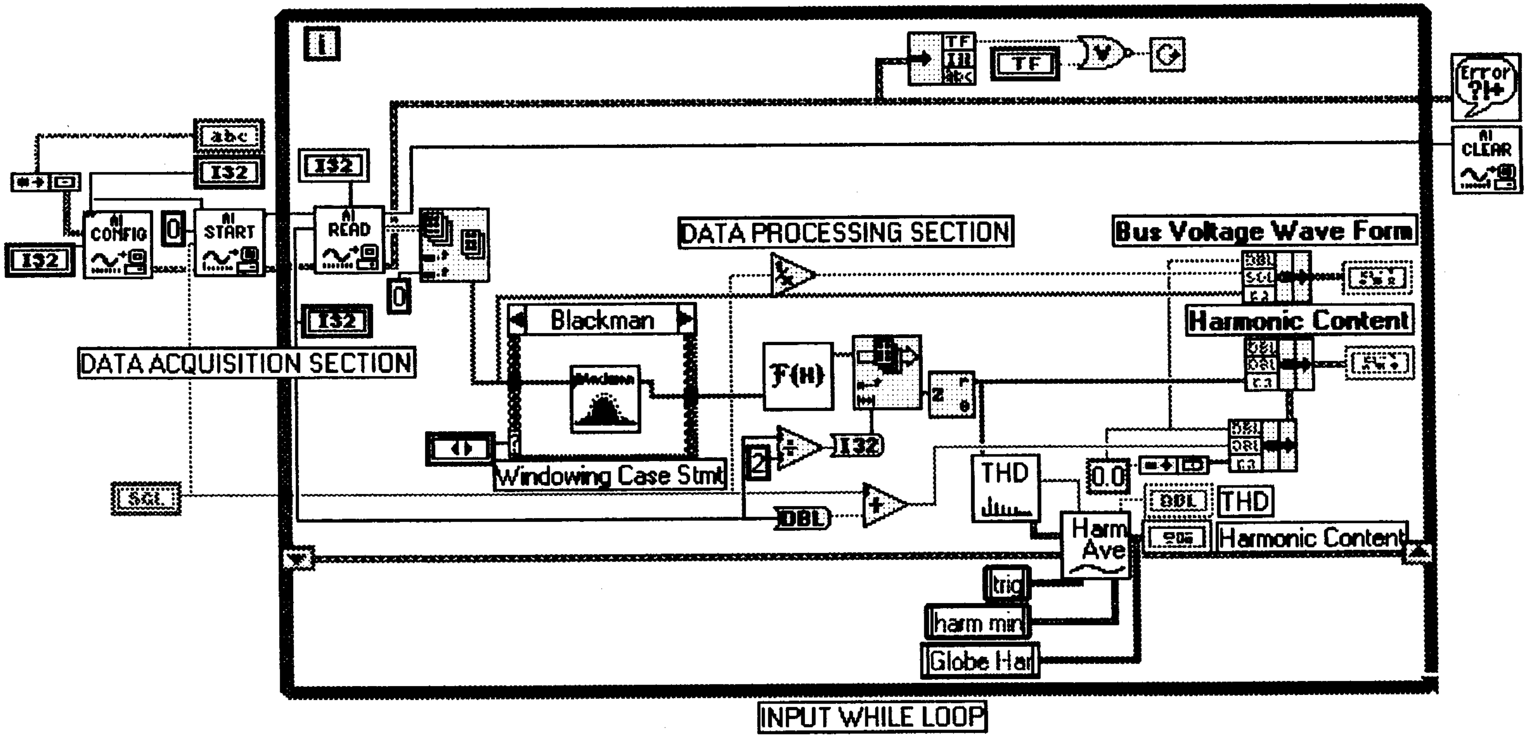

Figure 4.2 Data Acquisition and Data Processing

Hamming, Hanning, Blackman and Blackman-Harris windows were incorporated into *HARMONIC.VI*.

The digitally windowed array is passed to the DFT subVI. LabVIEW uses the Split-Radix FFT algorithm to compute the DFT when the array length is an integer power of two. The algorithm resembles the Radix-4 method but has the speed advantage of the Radix-8 method.[Ref. 10] The output of the DFT is an array of complex numbers containing the phase and magnitude information of the input arrays' spectrum. The magnitude of the spectrum is extracted and sent to the THD subVI.

The THD subVI computes the percent THD and scaled values of the energy contained in the harmonic frequencies. These scaled values are used in the control section as error signals. As discussed in Chapter III the THD of a periodic wave form is defined as the percent of the energy contained in the harmonics compared to that energy contained in the fundamental. Parseval's theorem states that the energy of a signal can be found by integrating the magnitude squared of the Fourier transform of the signal over all frequency. The energy contained within any bandwidth is determined by simply integrating the same argument over that frequency band. The THD subVI uses this and the information from the DFT to approximate the energy contained in the fundamental and harmonic frequencies.

The DFT is a sampled version of the discrete time Fourier transform (DTFT) taken of a sampled signal. Figure 4.3 shows graphically this concept. The horizontal axis is the discrete frequency corresponding to the fundamental and its 3rd and 5th harmonics. The approximation to the area underneath the squared DTFT for a given bandwidth is the squared DFT elements summed over the same bandwidth. The block diagram of the THD subVI is shown in Figure 4.4. The array entering this subVI is the magnitude of the DFT. The index of the array is related to the frequency of the signal. The subVI

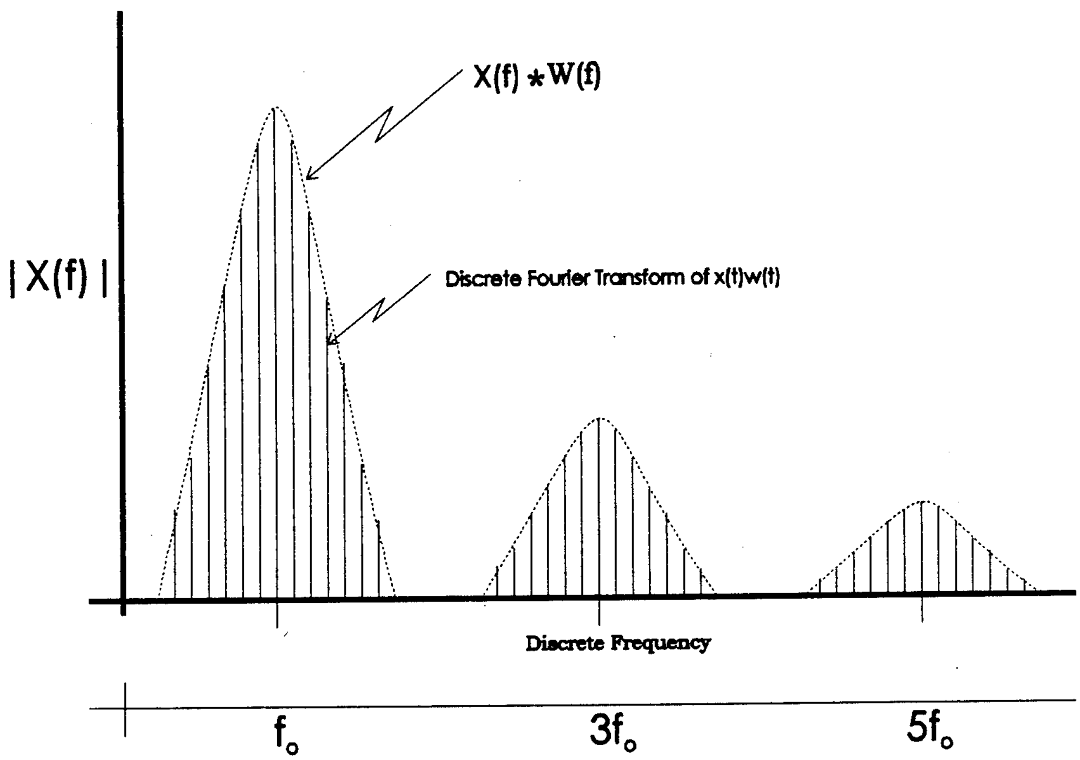

Figure 4.3 Graphical Representation of Discrete Fourier Transform

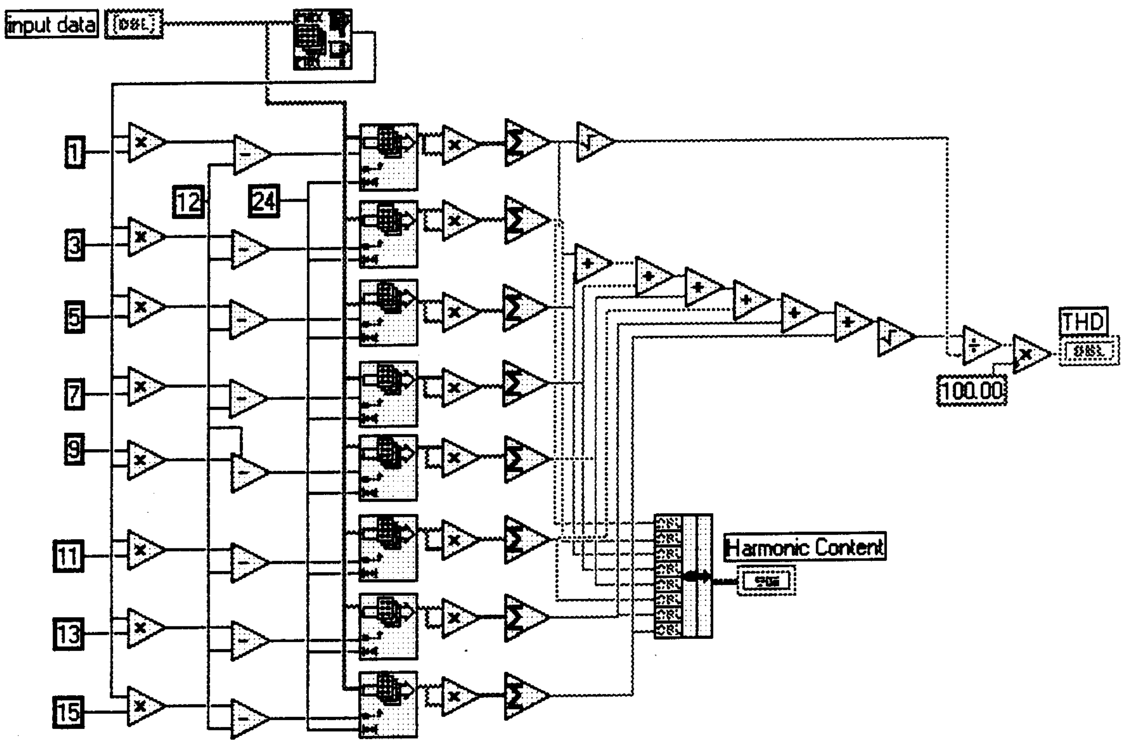

Figure 4.4 Block Diagram of THD subVI

determines the index containing the maximum value which corresponds to the fundamental frequency. The index of the harmonic frequencies is the fundamental index multiplied by the harmonic number. The array was split up into segments of twenty four elements centered at the indexes of the fundamental and harmonic frequencies. Each sub array was squared element by element and then summed to approximate a scaled value for the energy contained within the desired frequencies. THD was then calculated by taking the square root of the sum of the harmonic scaled values and dividing by the fundamental value. The scaling factor cancels out in the calculation of THD. The THD and scaled energy signals are then sent to the HARM AVE subVI.

The THD and error signals fluctuate making use of them for control difficult. HARM AVE subVI performs a weighting average of THD and the error signals. A block diagram of HARM AVE subVI is shown in Figure 4.5. The weights were picked to put more emphasis on the most recent values. In addition to the information provided for averaging this subVI receives a *trig* (trigger input) and *harm min* (harmonic min) from the control portion of *HARMONIC.VI*. Within this subVI a false *trig* input resets all the averaging elements to their minimum values *(harm min)* for control purposes. The information is displayed on the front panel and passed to the control section.

3. Control Development

Control development was the most challenging portion of the program. LabVIEW is a very powerful language for acquisition and processing but was not designed for control applications. The intent of the control section was to use the energy signal information from the processing section and derive the control signal weights mentioned in Chapter III. The control weights {S3,C3 ...Sh,Ch,...S15,C15} dictated the magnitude of the sine and cosines wave forms that were added together in order to produce harmonic

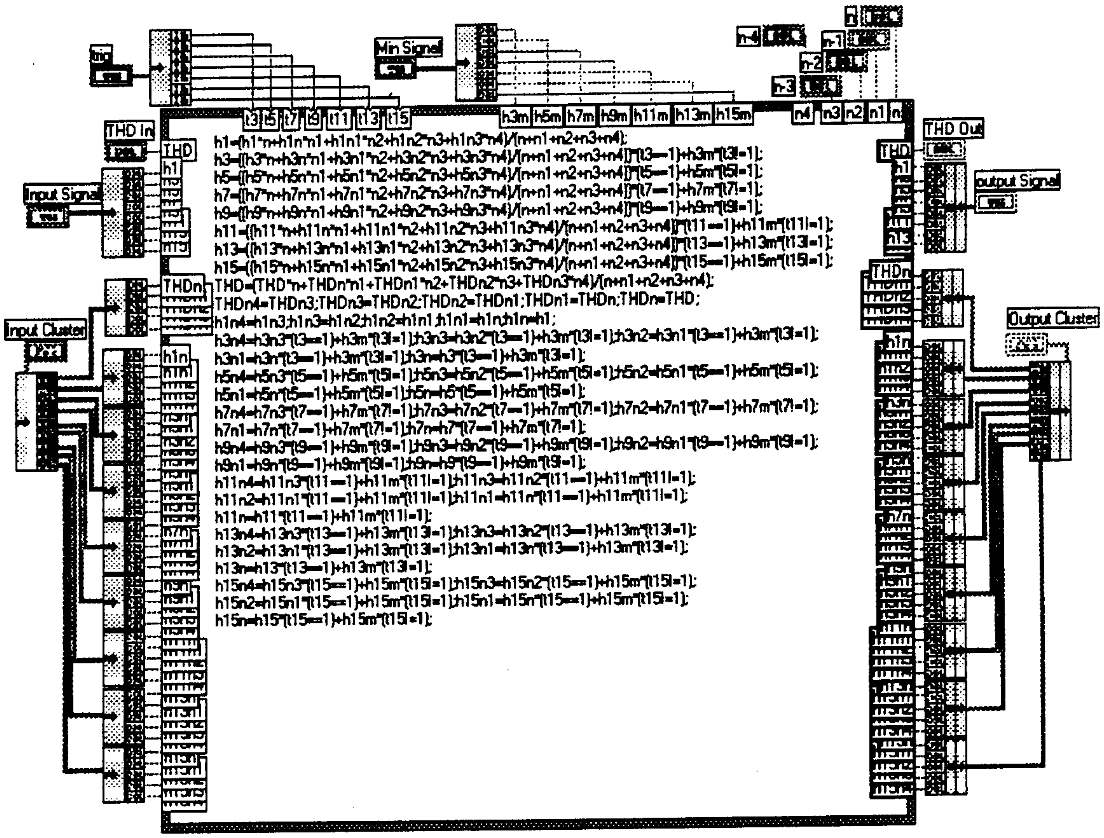

Figure 4.5 Block Diagram of HARM AVE subVI

canceling current signal which when injected into the network would reduce the energy contained in its corresponding harmonic.

Theoretically since the sine and cosine functions are orthogonal the correction signals proper phase and magnitude could be reached provided that the step size was small enough. The weights needed to be varied one at a time and the response of the system determined in order to see if the error signal had increased or decreased. Determining the gradient of the error as a function of the changing weight would dictate the direction that the weight would be varied. Once a minimum error signal was obtained the program could move on to the next weight. Implementing a state machine to sequentially control the distortion was decided to be the best approach. Figure 4.6 shows the state machine approach to the problem. The coupling effect between harmonics made parallel correction of harmonic to difficult.

Once the APLC was initialized and the control placed in *auto* the harmonic with the largest error signal would be selected. The weight of the sine component of the harmonic would start increasing. If the gradient were positive then the trigger would be false and the sine weight would be deceased. The weight would be continually decreased by a step size until the gradient turned positive and the trigger would become false. The state would continue to execute while the trigger was true or until control was shifted to *off, hold* or *manual*. The block diagram of the control case statements are shown in Figure 4.7. This sequence continues until the correction sequence is passed and the harmonic with the highest energy determined.

In practice, the gradient could not be easily used as the trigger because of fluctuations in the error signals. This problem was overcome by assigning a variable to store the lowest error signal value that occurs during each harmonics correction sequence and cause the trigger to become false when the error signal reached this minimum error

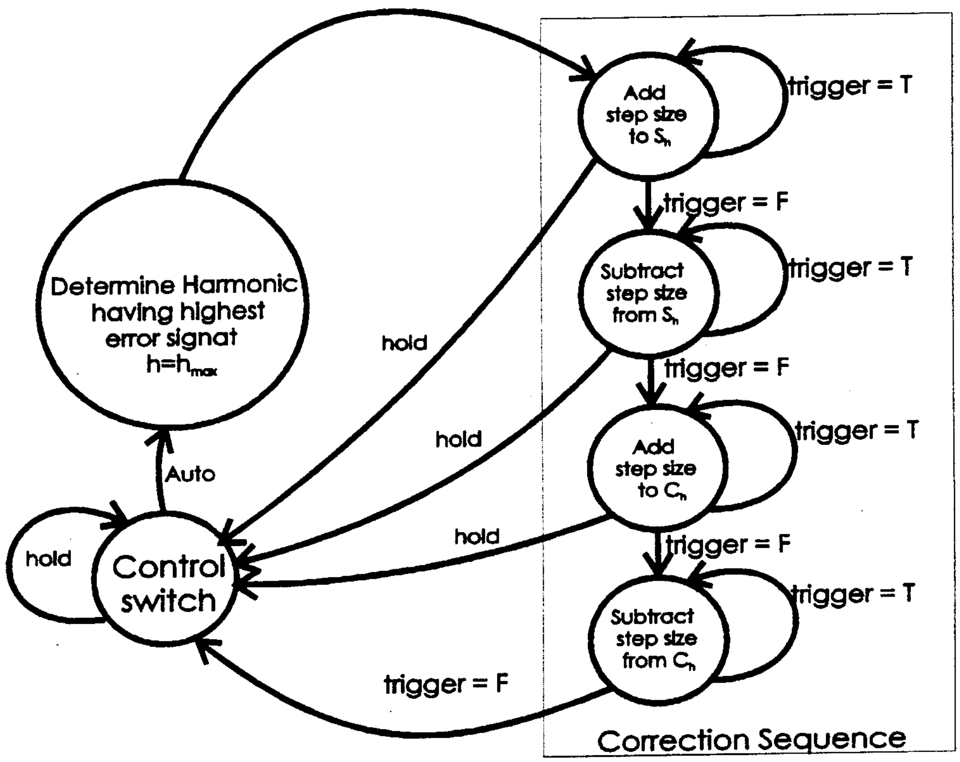

Figure 4.6 State Machine

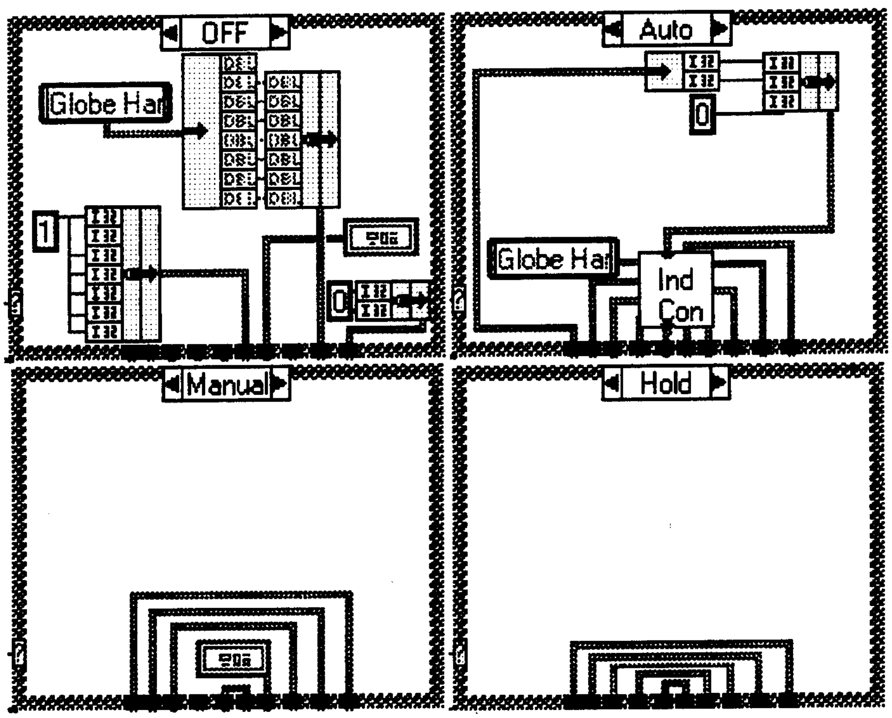

Figure 4.7 Control Case Statements

signal plus some offset. This in essence searched for the proper weights by "swinging or rocking" through the error signal. These are the *trig* (trigger input) and *harm min* (harmonic min) signals previously mentioned in the data processing section. Figure 4.8 shows the block diagram of the subVI used to control the APLC as described above. Each cycle the undated weights were sent to signal output section.

4. Signal Output

The AT-MIO-16F-5 data acquisition board has two analog output channels. Each channel has its own buffer that different data sequences can be stored. The board was set so that the conversion rate was constant. The output frequency could then be controlled by varying the number of cycles in the data sequence. Arrays containing sinusoidal (both cosine and sine) sequences, all of the same length, were generated in the SG subVI. The arrays each contained a different number of cycles. The odd harmonics were to be corrected therefore the arrays had the odd numbers as the number of cycles. Figure 4.9 shows the block diagram of the SG subVI. The weights developed in the control section were passed to the SG subVI to be the amplitudes of the arrays. The arrays are added element by element to develop the discrete distortion canceling signal. This signal is down loaded to the specified I/O channel of the data acquisition board to become the input of the current amplifier of the APLC.

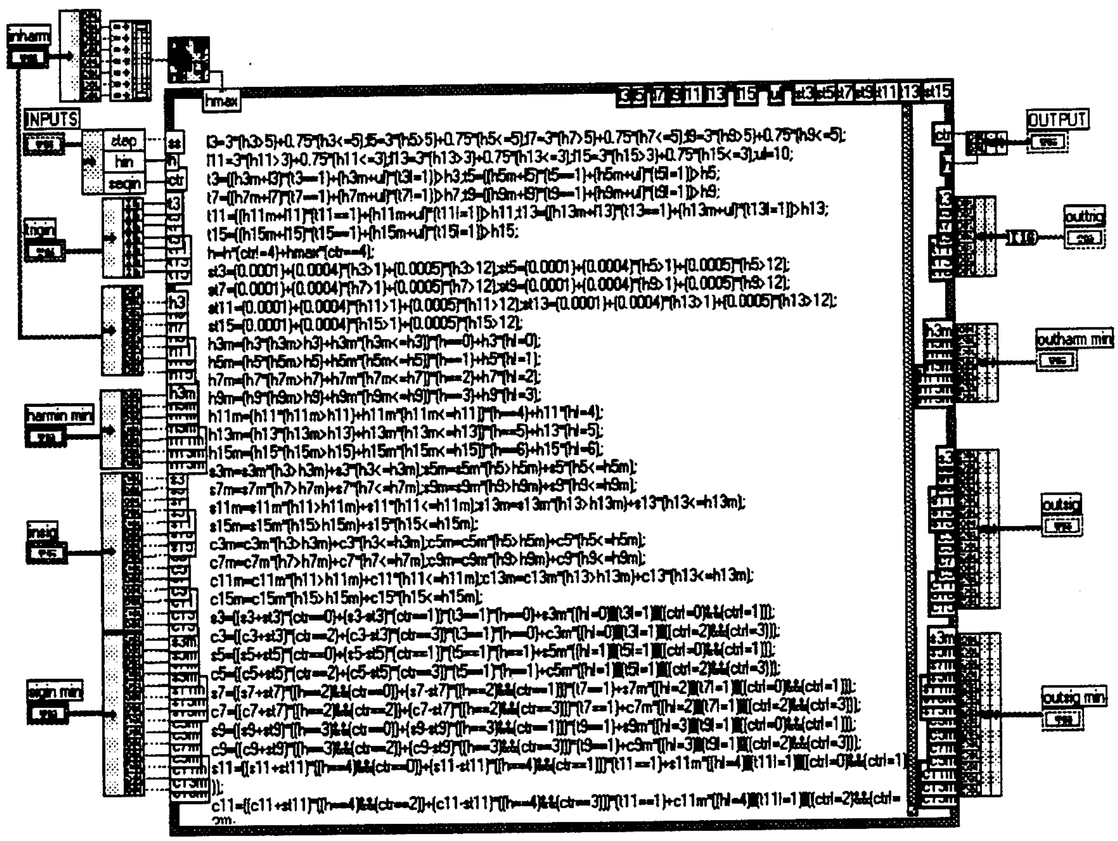

Figure 4.8 Block Diagram of Control subVI

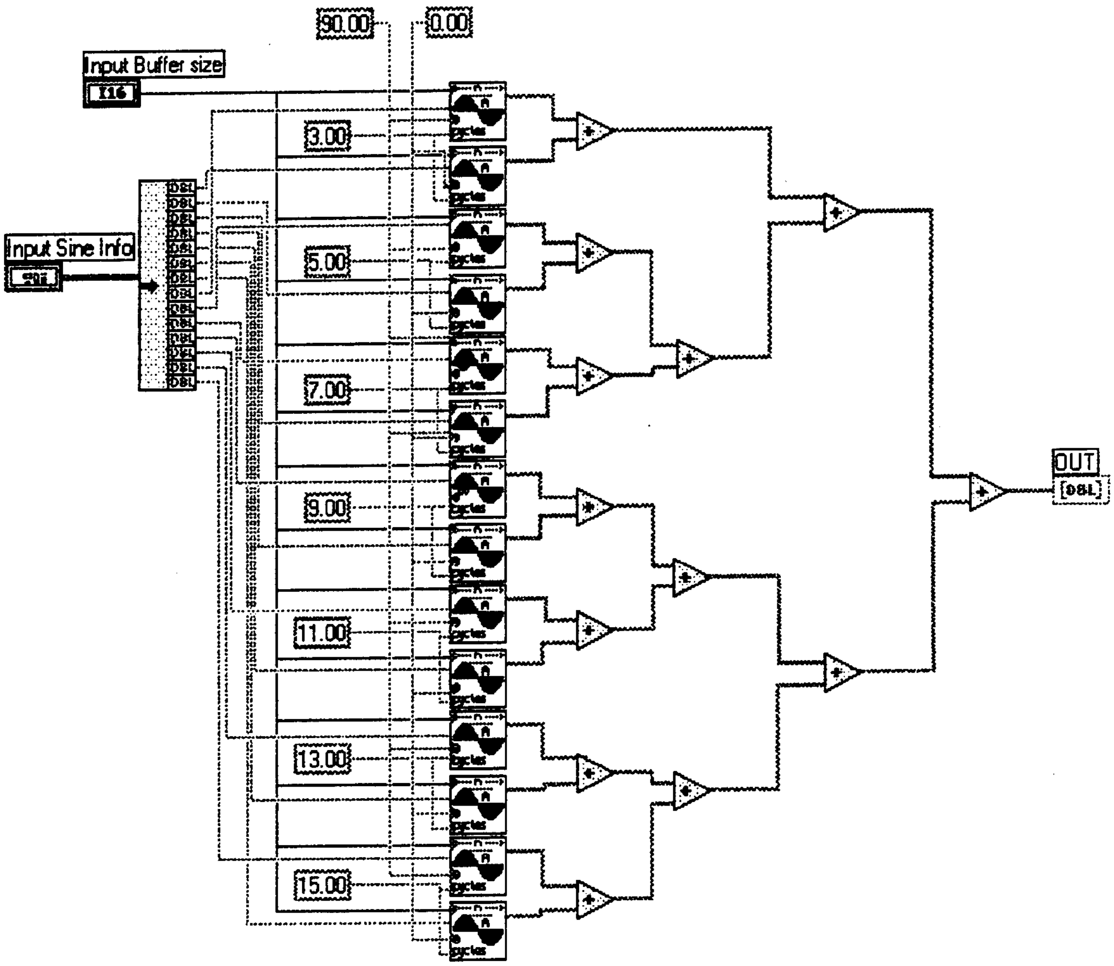

Figure 4.9 Block Diagram of Signal Generating subVI

V. ACTIVE POWER LINE CONDITIONER TESTING AND RESULTS

A. TEST SETUP

The diagram shown in Figure 5.1 depicts the testing and measuring setup for the APLC.

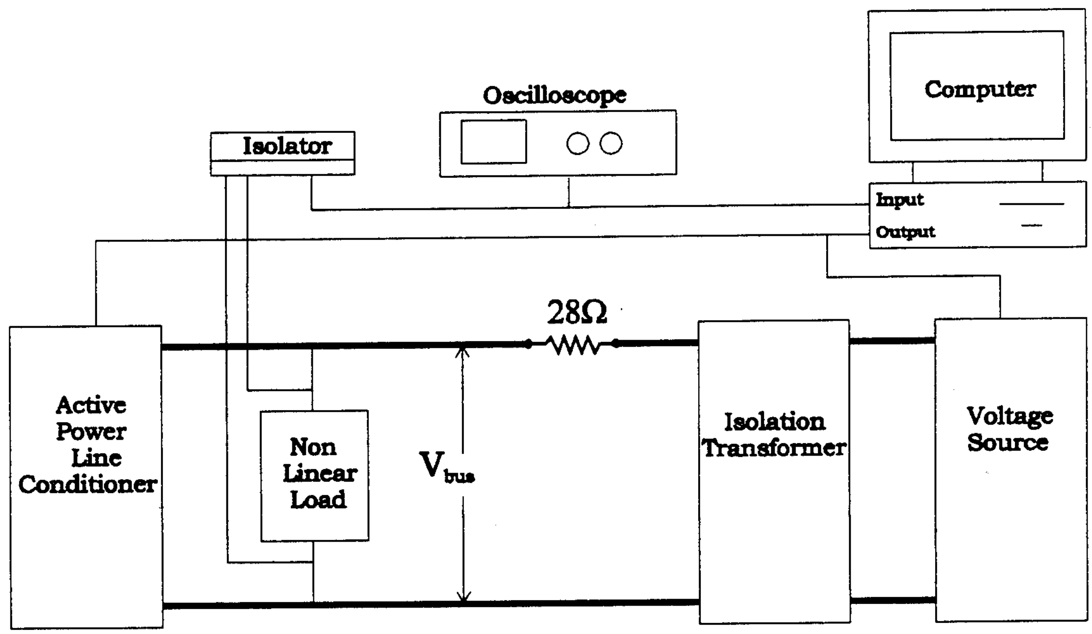

Figure 5.1 Testing and Measuring Setup

A Copley 262V amplifier, controlled by the computer, was operated as a voltage source. The amplifier was powered by the same source used by the current amplifier of the APLC and connected as described in Chapter III. The output voltage wave shape and frequency of the amplifier are controlled by the computer. This is done by utilizing the output of one of the data acquisition boards' D/A converters to drive the differential input to the amplifier. The voltage supply section of *HARMONIC.VI* generates a sinusoidal data array that is down loaded to the buffer associated with the specified I/O channel. The

conversion rate of the channels' D/A converter in conjunction with the number of periods of data contained in the I/O buffer controls the output analog frequency at the desired value. The Copley acts as an excellent low distortion voltage source with little associated output impedance. In addition there is no need for frequency synchronization since the computer is supplying the input sinusoidal signal for the amplifier. On the contrary, if building power were used, the line impedance and slowly varying frequency of the bus would need to be considered. For the purpose of this thesis, direct connection to the building was not advantageous to "proof of principle", but would only interfere with the accuracy by entering more unknowns unnecessarily.

The voltage source provided the power to the network as if it were supplied from an uncorrupted stiff power grid. The distortion on a local bus is caused by the voltage drop which occurs when the non-linear current drawn by the bus passes through the transmission line. The line resistor (28Ω) and the isolation transformer performed the part of the transmission line.

The test equipment is powered by the wall outlet and therefore grounded. The output of the Copley amplifiers need to be ungrounded; the test circuit was therefore made to float. The Tektronix A6902B isolator isolated the ungrounded test circuit from the test equipment. An additional reason for using this type of isolator was its ability to step signals down. The voltage was reduced to meet the dynamic range of the data acquisition boards' converters.

The non-linear load used in the test circuit was an inductor in series with a parallel connected capacitor and resistor, all of which were driven by a phase controlled rectifier (PCR). The test circuit is shown in Figure 5.2. The firing angle of the PCR is adjustable by a precision potentiometer on the Variable AC/DC Supply Logic box. By adjusting the firing angle, the amount of fundamental and harmonic current drawn were varied.[Ref. 11]

The ability to finely control the total amount of current drawn from the "weak" bus allowed the for precise regulation the THD of the bus voltage.

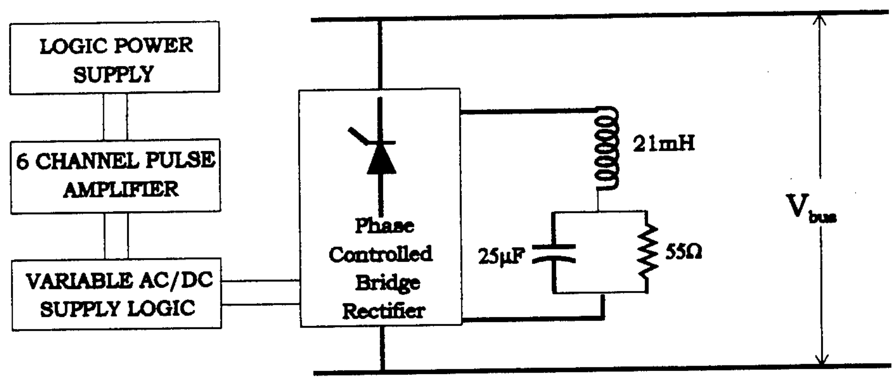

Figure 5.2 Non-linear Load

The following procedure is used for readying the test circuit for evaluation.

1. Energize computer, oscilloscope and isolator.
2. From the 208 VAC supply energize the rails of the amplifiers. Use the variac and adjust the rail voltage to at least 150VDC.
3. Provide power to the PCR by energizing the Logic Power Supply, 6 Channel Pulse Amplifier and Variable AC/DC Supply Logic, in this order.
4. At the computer, execute the LabVIEW program from Windows.
5. In LabVIEW, execute the *HARMONIC.VI*.
6. Using the mouse start the VI running. The default values in the VI will energize the voltage source and start acquisition of bus voltage data.

The VI takes a finite number of cycles to load the averaging elements. The elements are fully loaded when the THD fluctuates less than one percent. Once the THD is relatively stable the system is initialized and ready to be placed in *auto* for control to

begin. The APLC continues to correct the distortion until the control selector is shifted to *off* or *hold*.

B. RESULTS

The trial run presented in this thesis started at a realistic distortion level of 12.5 percent. Figure 5.3 shows the initial distorted bus voltage wave form and the spectrum of harmonic energy. The spectrum is automatically scaled in the vertical direction but fixed in the horizontal direction. The x-axis starts at 100 Hz instead of the typical 0 Hz to cut out the fundamental energy spike. The energy of the fundamental is many orders of

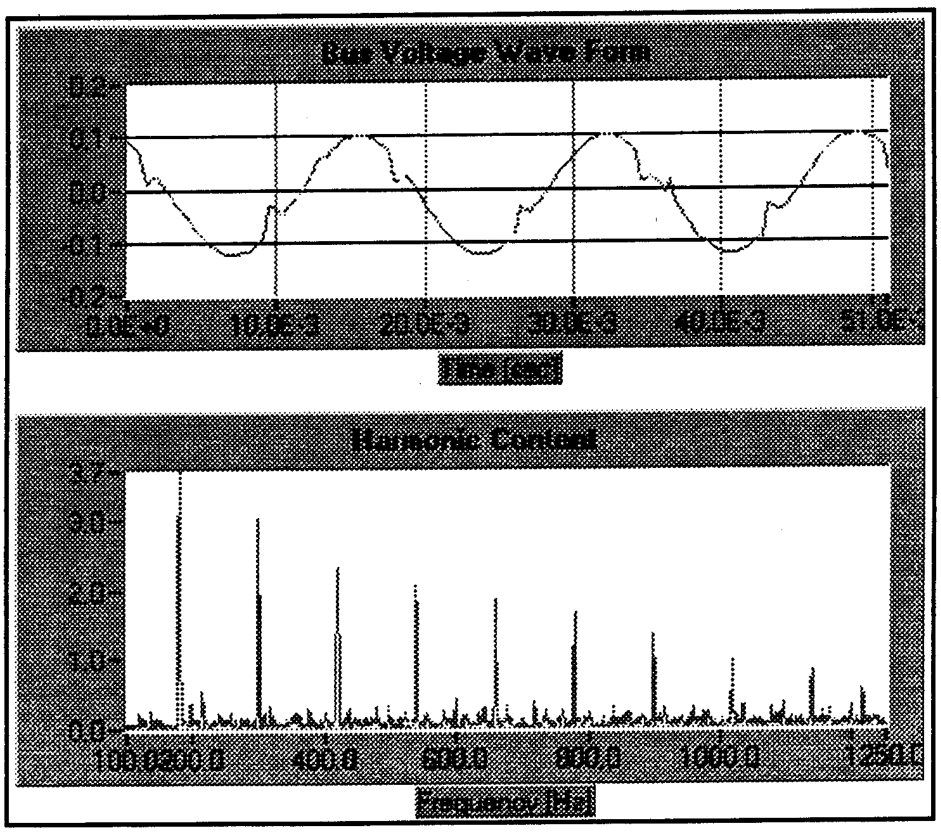

Figure 5.3 Bus Voltage and Energy Spectrum

magnitude larger than its harmonics and would overshadow their presence on the spectrum.

The corrected bus voltage wave shape and its associated spectrum is shown in Figure 5.4. The obvious notch that was present in the uncompensated wave shape has been essentially eliminated. The compensated wave shape has significantly improved towards the desired sinusoid. The spikes that are still present in the compensated voltage wave shape are due primarily to the harmonics that were higher than the 15th which were not corrected. The spectrum shows that the uncorrected harmonics' energy has increased due mainly to the coupling effect of the non-linear load. The final THD was 3.0 percent.

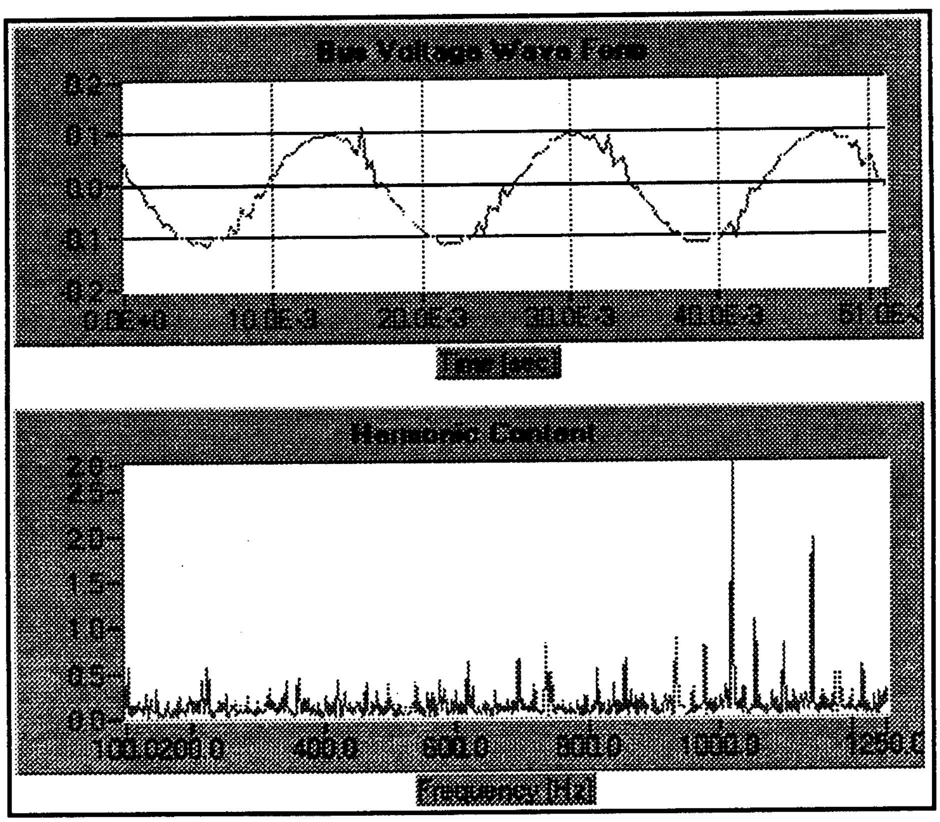

Figure 5.4 APLC Corrected Bus Voltage and Energy Spectrum

The decrease in percent THD during the trial run is shown Figure 5.5. During testing it became very apparent that the convergence rate to the proper control weights and hence the drop of THD were sensitive to step size, averaging technique, data windowing and triggering levels. Figures 5.6 through 5.12 show the variations of each of the corrected harmonics' error signal and weights over time. As explained in Chapter IV, sequential control was used to remove the harmonic distortion. The harmonic with the highest error signal is corrected first. The periods that the weights are not varying are the times that some other weight is being changed either in the same harmonic or another with a larger error signal. At times when the weights of a particular harmonic are not being changed yet its' error signal is increasing, Figure 5.8 through 5.12, shows the significant amount of coupling that exists between harmonics. As expected the weights were converging on unique values depending of the network topology.

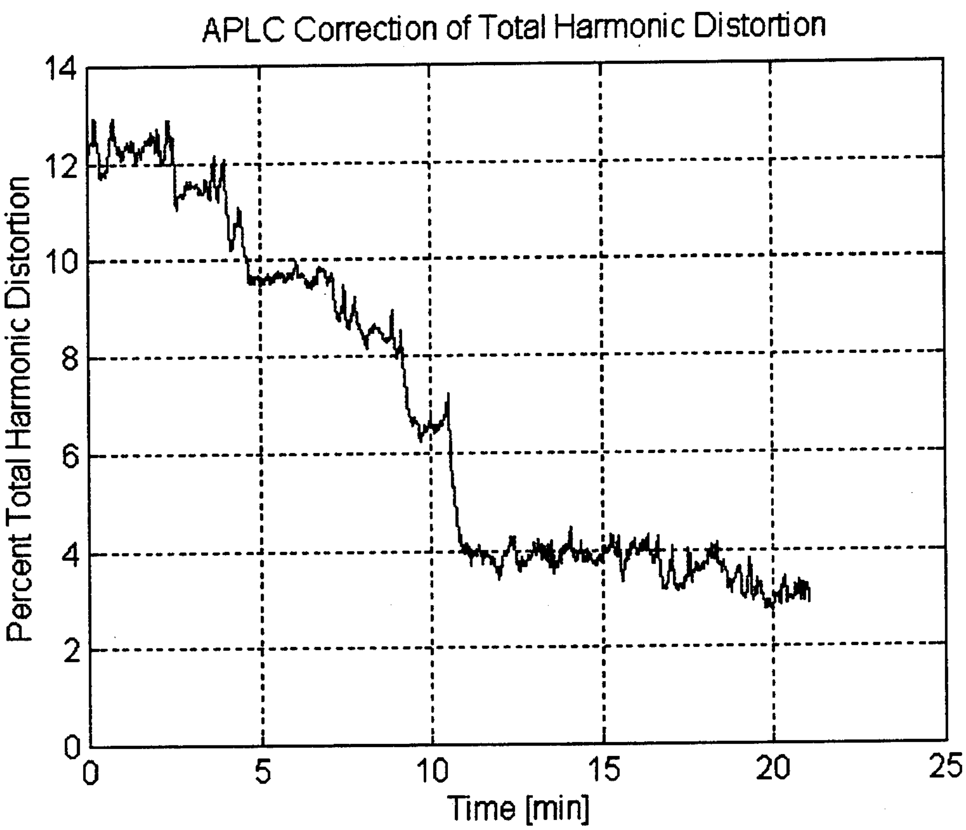

Figure 5.5 Percent THD of Bus Voltage Over Time

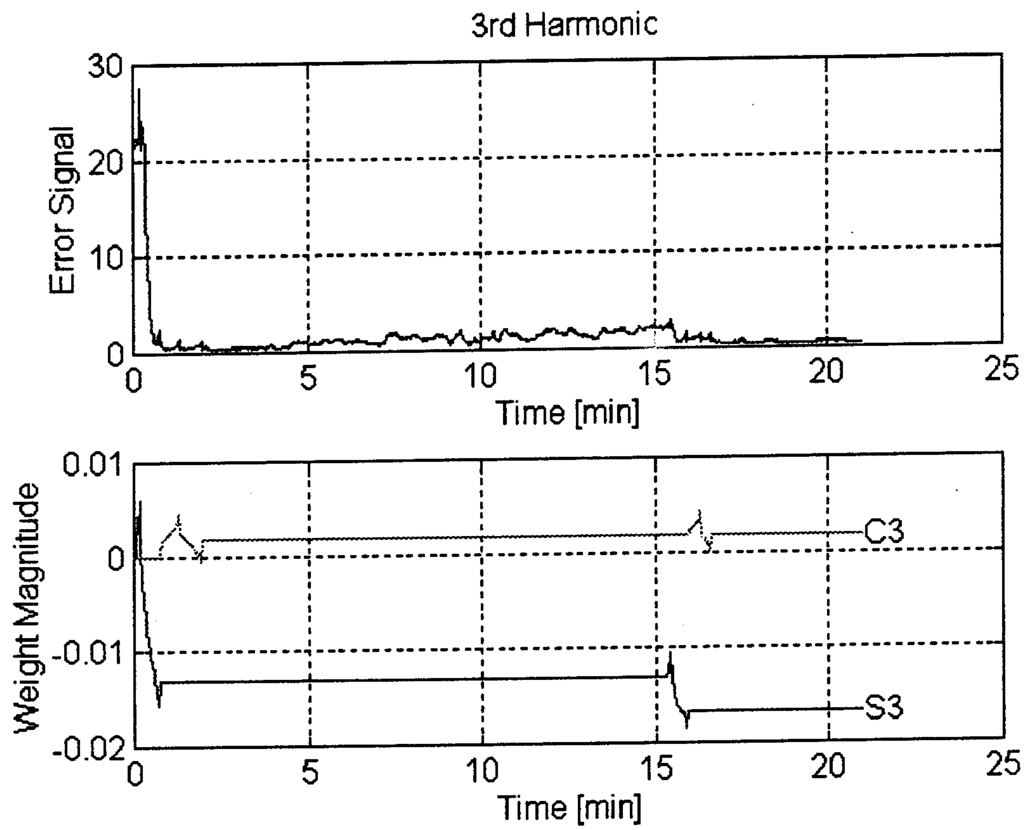

Figure 5.6 3rd Harmonic Error Signal and Weight Magnitudes Over Time

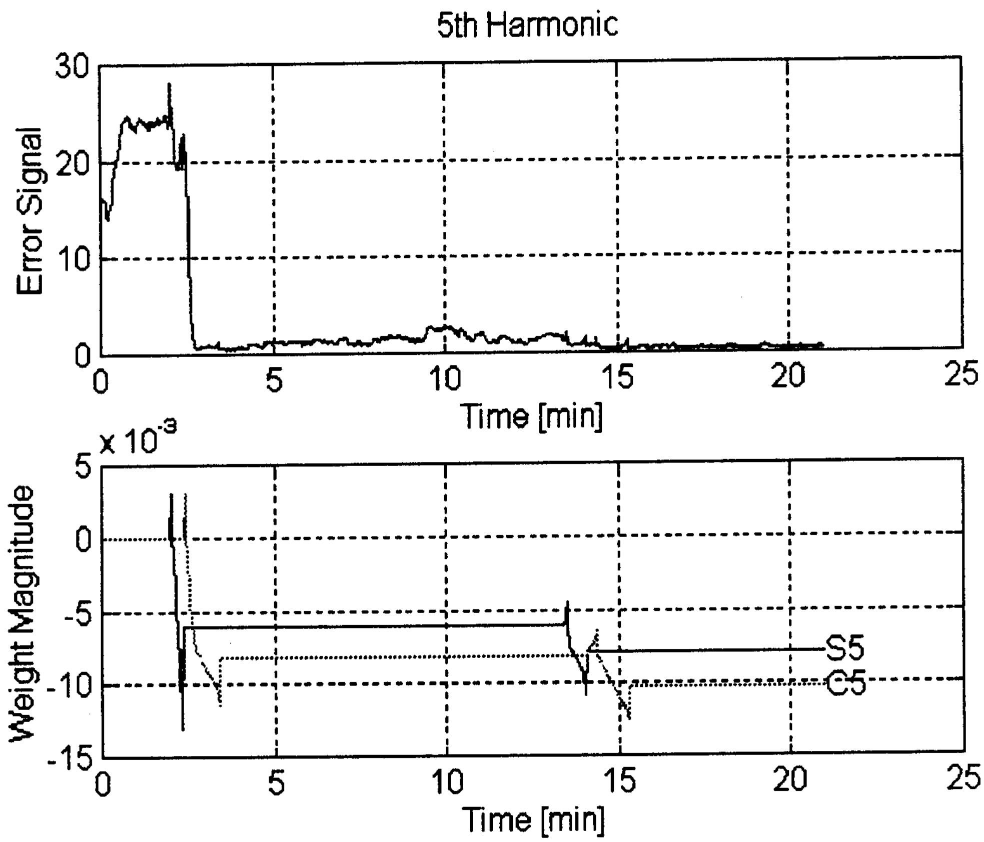

Figure 5.7 5th Harmonic Error Signal and Weight Magnitudes Over Time

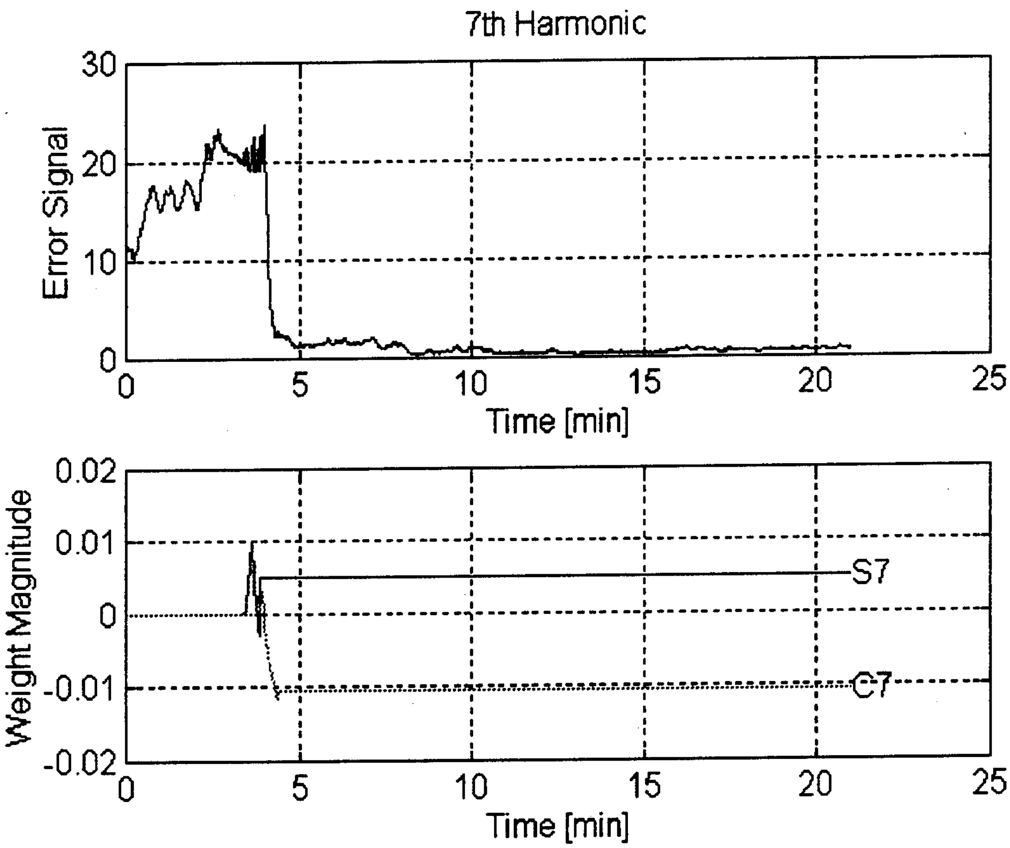

Figure 5.8 7th Harmonic Error Signal and Weight Magnitudes Over Time

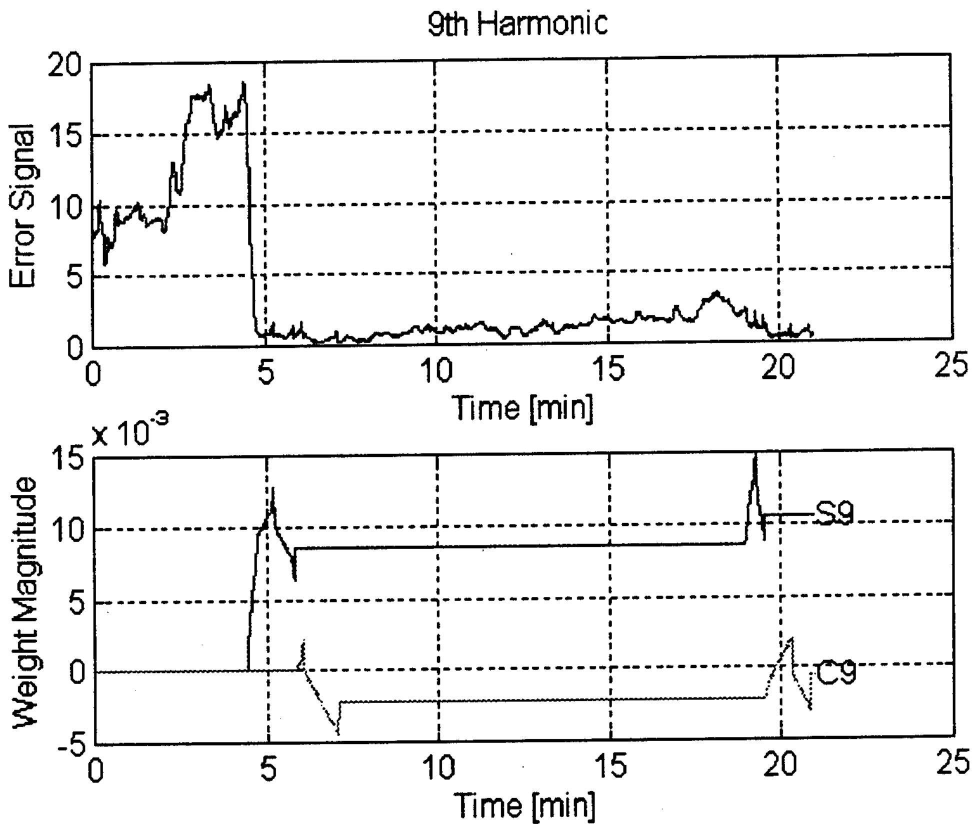

Figure 5.9 9th Harmonic Error Signal and Weight Magnitudes Over Time

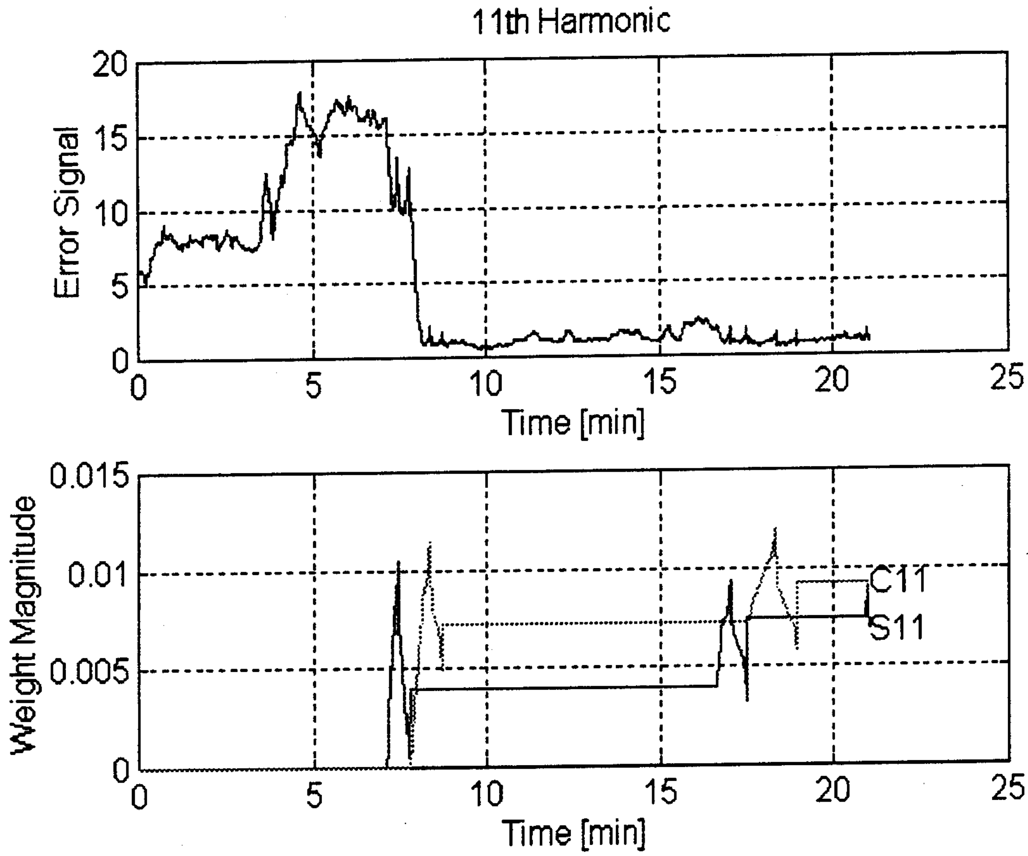

Figure 5.10 11th Harmonic Error Signal and Weight Magnitudes Over Time

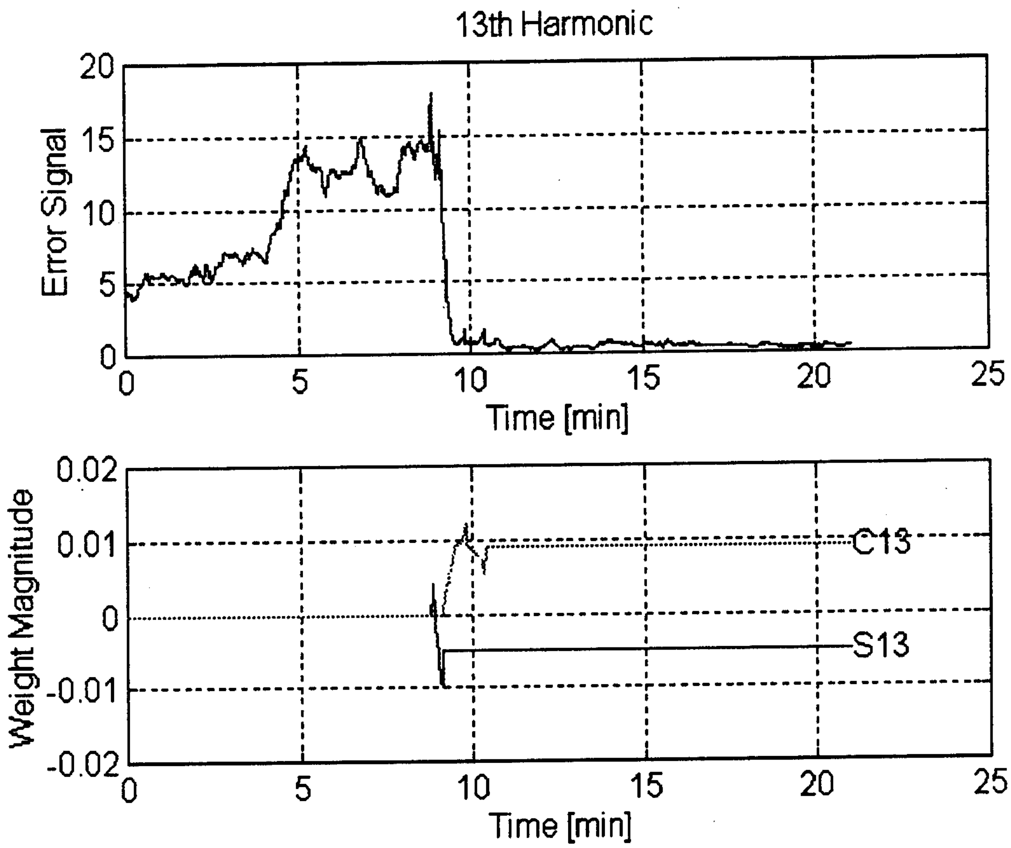

Figure 5.11 13th Harmonic Error Signal and Weight Magnitudes Over Time

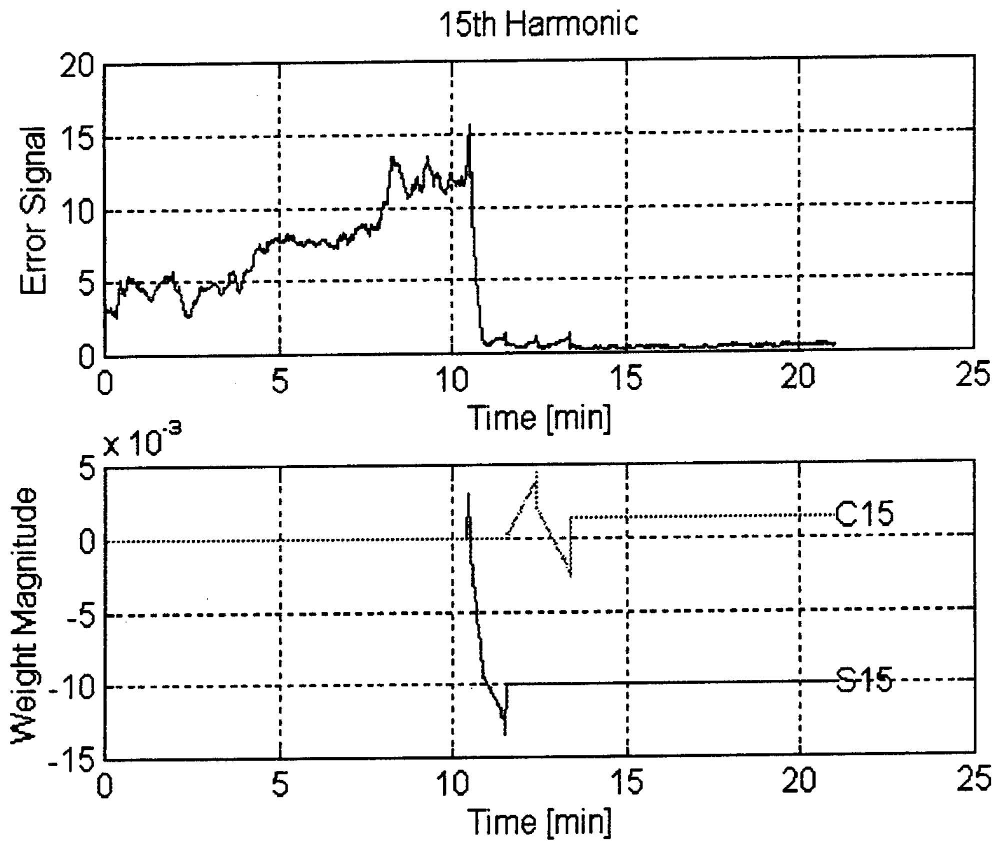

Figure 5.12 15th Harmonic Error Signal and Weight Magnitudes Over Time

VI. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The main goal of this thesis was to prove that THD of a local bus could be corrected using only the knowledge of the local bus voltage. To this end, the results presented in Chapter V show that the APLC, controlled solely from information derived from the bus voltage, reasonable reduced the THD at the bus. The shortcoming indicated by the results was the length of time that the algorithm took in order to come up with the correct weights.

A secondary goal of the thesis was to create an optimal algorithm for determining the control weights. The coupling that existed between harmonics led to a sequential approach. This significantly contributed to the time required to reduce the THD. Since both the phase and magnitude of the correction signal were unknown, only one of the orthogonal functions could be varied at a time; this dictated a sequential approach to each harmonic which added additional time to the process. The algorithm presented in this thesis gave the best results considering the coupling effects and the limitation of LabVIEW as a controller.

B. RECOMMENDATIONS

Implementation of this approach on a dedicated digital signal processor (DSP) board, such as the TMS520C30, should be investigated. The versatility of the C programming language and the capability of today's DSP boards would allow for easy implementation and compactability of the process.

The time to reduce the THD could be improved if *a prior* knowledge of the network was known. The changes in a distribution system topology is periodic to some extent. A neural network could be trained for a given system to predict its impedance matrix, thus providing a starting point to the APLC. Additionally, the APLC could be used to collect the information for the neural network since it would require injecting various currents and monitoring the corresponding changes in bus voltage to determine this impedance matrix.

A unity power factor converter should be built to provide the power to the APLC. This converter could be powered off the same bus. This would close the loop and theoretically make it feasible to install this type of self-contained harmonic correction device in to any system with only one tap-in point.

LIST OF REFERENCES

1. Grady, W.M., Noyola, A.H., and Samotyj, M.J., "Survey of Active Power Line Conditioning Methodologies," *IEEE PES*, Winter Meeting, Atlanta, GA, February 4, 1990.

2. Henderson, R.D., and Rose, P.J., "Harmonics: The Effects on Power Quality and Transformers," *IEEE Trans. on Ind. Apps.*, Vol. 30, No. 3., pp528-532, May/June 1994.

3. Mohan, N., Undeland, T., and Robins, W., *Power Electronics, 2nd Edition*, John Wiley & Sons, Inc., New York, NY, 1995.

4. Reid, W.E., "Power Quality Issues-Standards and Guidelines," *IEEE Trans. on Ind. Apps.*, pp108-115, June 1994.

5. *Operating and Service Manual Models 232, 232V, 262, and 262V High Power Amplifier*, Copley Controls Corp., Westwood, MA, August 1993.

6. *AT-MIO-16F-5 User Manual*, National Instruments, Austin, TX, July 1993.

7. Ashton, R.W., *Harmonic and Power Factor Correction By Means of Active Line Conditioners With Adaptive Estimation Control,* Ph.D. Dissertation, Worcester Polytechnic Institute, Worchester, MA, 1991.

8. *DataStor Deskside Computer*, Data Storage Marketing, Inc., Boulder, CO, 1993.

9. *LabVIEW for Windows User Manual*, National Instruments, Austin, TX, December 1993.

10. *LabVIEW Analysis VI Reference Manual*, National Instruments, Austin, TX, August 1993.

11. Fisher, M.J., *Power Electronics*, PWS-KENT Publishing Co., Boston, MA, 1991.

INITIAL DISTRIBUTION LIST

1.	Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2.	Library, Code 52 Naval Postgraduate School Monterey, California 93943-5101	2
3.	Chairman, Code EC Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
4.	Professor Robert W. Ashton, Code EC/Ah Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
5.	Professor Michael K. Shields, Code EC/Sl Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
6.	Professor Gurnam S. Gill, Code EC/Gl Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
7.	Lt. Kevin Jones c/o Ted Kyle 2428 Hickory Valley Rd Chattanooga, Tennessee 37421-1721	2